Computational Prediction of Lithography DTCO for Ultra-low power AI-Edge Chips

Kazuya Kadota, NanoscienceLab., e-mail: drkadota@hotmail.co.jp

With the advent of artificial intelligence age, the need for ultra-fine devices has been expanded to AI-edge chip applications and has become an important position as the leading-edge industry. In previous research, H. Fuketa et al., have conducted detailed research and development aimed at ultra-low power consumption for 65nm nodes from the circuit and device perspectives[1].

This paper is researched from the viewpoint of DTCO (Design Technology Co-Optimization) in the lithography field, because the future AI-edge chips will inevitably move toward higher integration and sub-nanometer lithography. Computational prediction on the device performances was performed with the target of cache SRAM for the ultra-low power consumption.

Specifically, the electronic characteristics (Standard CMOS, Vdd, SNM, Vth, I-V, etc.) of the cache SRAMs composed a gate length of 16 nm Node 6 Fin-type transistors were calculated and predicted by TCAD (HyENEXSS™ was used)[2]. From the lithography perspective, first, the electronic characteristics were calculated and predicted by applying the Single Pattern Technology (SPT) by immersion exposure that is most advantageous for productivity. Tachyon™ was applied as the lithography calculation simulator. However, in particular on SPT, EPE (Edge Placement Error) has a great influence on electronic characteristics and ultra-low power consumption, and it was found that there are instability factors in the operation of SRAM.

On the other hand, it was examined the Quadrupole Pattern Technology (QPT) which made closely to the original design layout pattern as similar as possible, and that greatly improved this EPE shape. Figure.1 shows the power supply voltage (Vdd) computer prediction results which the overlay error were intentionally applied on each transistor during the SPT and QPT computation, and shows Vdd is extremely enhanced. Depend on the intentional overlay error, the stable region of Vdd is narrow in the SPT case, but in the QPT, it was found that Vdd stably expands to 0.4V or 0.3V.

As a result, the power supply voltage (Vdd), which is the key to stable operation at ultra-low power consumption, can be reduced to 0.3V or 0.4V, and it means the operational energy can be saved to be about 9% or 16% relatively. This computational prediction result is extremely useful for the future realization and application for the AI-edge chips.

References:
1) H. Fuketa., et.al; IEDM-2011 S25P01, Y. Yamamoto., et.al; VLSI-2013 T212.
2) K. Kadota et.al; IEICE-1985, SPIE-922 (1988), SPIE-1088 (1989), PMJ-2011, PMJ-2013, PMJ-2016, MNC-2011, JSAP-2016, JSAP-2017, NGL-2017, JSAP-2018, NGL-2018, JSAP-2019, NGL-2019.

Acknowledgment:
This research is part of the result of the joint research with National Institute of Advanced Industrial Science and Technology. I express my gratitude to everyone concerned.

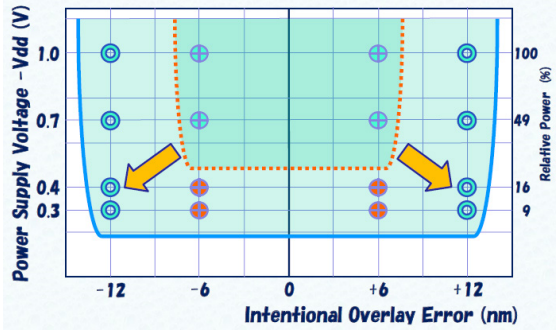

Figure-1. Relation between Vdd and intentional overlay error.