SOI 細線アレイ上への低転位 Ge 層のエピタキシャル成長

Ge epitaxial layer with a low dislocation density grown on arrayed SOI strips

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1. Introduction

Selective epitaxial growth of Ge layer on a Si-on-insulator (SOI) wafer has been used in the fabrication of near-infrared photodetectors in Si photonics [1]. A high-quality Ge layer is required for the high-performance devices despite a large lattice mismatch of 4% between Ge and Si. We have reported that the threading dislocation density (TDD) is significantly reduced in a coalesced layer of Ge selectively grown on a bulk Si wafer with an array of strip-patterned SiO_2 masks [2]. The TDD reduction is derived from a downward bending of the dislocation, which is penetrated to the surface of void overlying the SiO_2 masks [2]. In this work, a coalesced layer of Ge is studied, which is grown on an array of strip-patterned SOI layers.

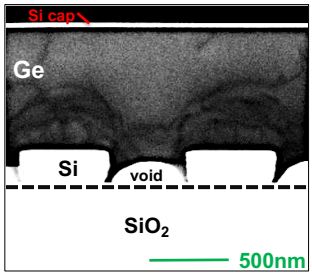
2. Experimental procedure

Using a photolithography and a dry etching, the top Si (001) layer (250 nm in thickness) of an SOI wafer was patterned into a periodic strips running in the [110] direction. The strip width was changed as a parameter (0.3 μm, 0.5 μm, and 1.5 μm). On the other hand, the spacing (0.5 μm) was fixed between the strips, where the surface of the buried SiO_2 layer was exposed. Then, a 1-μm-thick Ge layer was epitaxially grown by ultrahigh vacuum chemical vapor deposition at 700˚C using a source gas of GeH_4. The structures were evaluated by cross-sectional transmission electron microscopy (TEM).

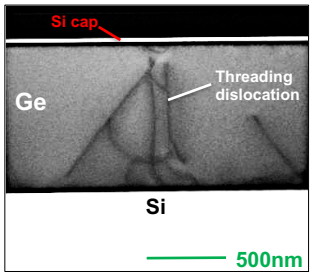
3. Results and discussion

Fig. 1(a) shows a typical cross-sectional TEM image of a Ge layer grown on an array of 0.5-μm-wide SOI strips. A continuous layer of Ge with a flat surface was formed, although the bottom SOI layer was not a continuous film. Voids were left on the exposed SiO_2 surfaces between the SOI strips. This indicates that the Ge growth was suppressed on the sidewalls of the SOI strip as well as on the exposed SiO_2 surfaces, while the growth preferentially took place on the top surfaces of the SOI strip, followed by a lateral growth to form the coalesced layer.

Dislocations were observed in the coalesced Ge layer, which mostly bent downward, i.e., semicircular-shaped dislocation bundles were present above the SOI strips. A part of the dislocations penetrated to the bottom void surfaces, similar to Ref. [1], while the other dislocations were accumulated near the sidewalls of the SOI strips. This is considerably different from the Ge layer on an unpatterned one in Fig. 1(b), where the dislocations were penetrated to the top surface. The downward bending should be effective to reduce TDD. In fact, the TDD in the coalesced Ge layer was found to be smaller than that for Ge on the unpatterned one, according to the etch-pit density measurement.



(a) Strip-patterned SOI



(b) Unpatterned SOI

Fig. 1. Typical cross-sectional TEM images.

4. Summary

Ge was grown on an array of strip-patterned SOI layers. A continuous layer of Ge with a flat surface was formed, where voids were left on the exposed SiO_2 surfaces between the SOI strips. Dislocations showed a downward bending, leading to a TDD reduction.

Acknowledgement

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[1] J. Michel et al., Nature Photon. 4, 527 (2010).
[2] M. Yako et al., J. Appl. Phys. 128, 185304 (2018).