SiO_2 犠牲層プロセスを用いた厚み 10 nm 以下の SiN ナノポアメンブレンの形成

Sub-10-nm-thick SiN nanopore membranes fabricated using the SiO_2 sacrificial layer process

日立研開　○柳　至，武田　健一

Research and Development Group, Hitachi Ltd., Itaru Yanagi and Ken-ichi Takeda

E-mail: itaru.yanagi.yr@hitachi.com

In our previous studies, ultrathin SiN membranes down to 3 nm in thickness were fabricated using the poly-Si sacrificial layer process [1], and nanopores were formed in those membranes. The region of the SiN membrane fabricated using this process was small, and the poly-Si sacrificial layer remained throughout the other region. On the other hand, to reduce the noise of the current through the nanopore, it is preferable to reduce the capacitance of the nanopore chip by replacing the poly-Si layer with an insulator with low permittivity, such as SiO_2. In this study, fabrication of SiN membranes with thicknesses of 3-7 nm using the SiO_2 sacrificial layer process was demonstrated. Nanopores were then fabricated in the membranes via dielectric breakdown. The current noise of the nanopore membranes was approximately 3/5 that of membranes fabricated using the poly-Si sacrificial layer process. In addition, ionic current blockades were measured when poly$(dT)_{60}$ passed through the nanopores, and the effective thickness of the nanopores was estimated based on those current-blockade values. The effective thickness was approximately 4.8 nm when the actual thickness of the SiN membrane was 6.03 nm. On the other hand, the effective thickness and the actual thickness were almost the same when the actual thickness was 3.07 nm. This may suggest the difficulty of forming the shape in which the membrane was thinner only near the nanopore than in the other area as the actual thickness decreased.

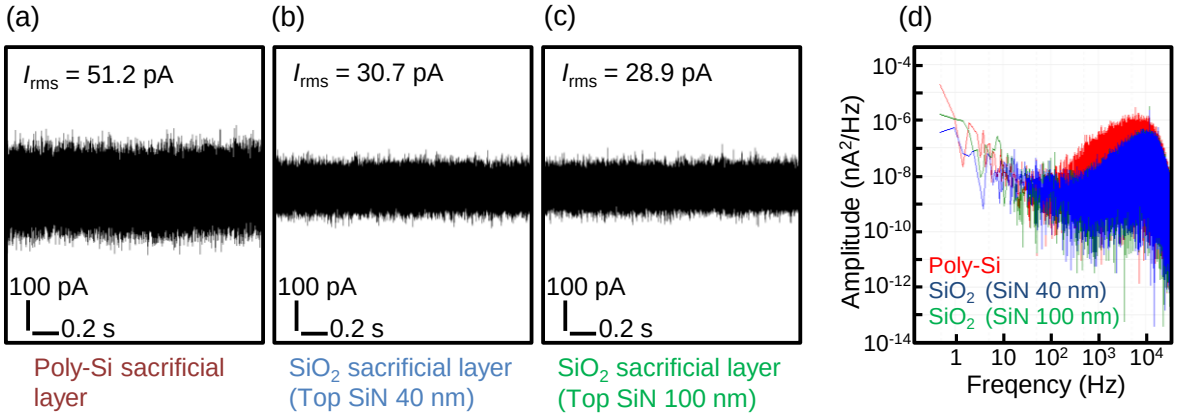

Figure 1. (a)-(c) Ionic currents through nanopore membranes fabricated with the poly-Si sacrificial layer, the SiO_2 sacrificial layer with the 40-nm-thick top SiN layer, and the SiO_2 sacrificial layer with the 100-nm-thick top SiN layer. The voltage applied was 0.1 V. The thickness of the membranes was approximately 5 nm. (d) Noise power spectra of the currents though the nanopore membranes fabricated using the three different processes.

Reference
[1] Yanagi, I., Ishida, T., Fujisaki, K. & Takeda, K. *Sci Rep* **5**, 14656 (2015).