C-V 測定による Al_2O_3/GeO_x/p-Ge MOS 界面の電子とホールの遅い準位密度の評価

Evaluation of electron and hole slow trap density in Al_2O_3/GeO_x/p-Ge gate stacks by C-V measurements

◦柯 夢南[1], 竹中 充[2], 高木 信一[2]
1. 東理大・工 2.東大院・工
[O]M. Ke[1], M. Takenaka[2], and S. Takagi[2]
1. Tokyo University of Science, Faculty of Engineering 2. The University of Tokyo, School of Engineering
E-mail: mke@ee.kagu.tus.ac.jp

Introduction A critical issue of Ge as a next generation channel material for CMOS devices is the formation of the high-quality gate stacks. Here, Al_2O_3/GeO_x/Ge and $HfO_2/Al_2O_3/GeO_x$/Ge structures realized by plasma post oxidation with 1 nm or thinner EOT and low D_{it} of ~10^{11} $eV^{-1}cm^{-2}$ are the promising gate stack structures [1-2]. However, one of the remaining problems is the existence of a large amount of slow traps [3-6]. We have proposed an evaluation method of slow traps to use hysteresis of C-V curves for GeO_x-based n-Ge MOS interfaces [7] and have reported several methods for slow trap density (ΔN_{st}) reduction in n-Ge MOS interfaces [8-9]. However, ΔN_{st} of GeO_x-based p-Ge MOS interfaces have not been fully studied yet. In this study, ΔN_{st} evaluation by using hysteresis of C-V curves has been performed for Al_2O_3/GeO_x/p-Ge MOS interfaces. It is found through careful examination of the C-V hysteresis that slow trapping under a small positive gate bias ($<V_{th}$) is attributed only to hole trapping. Under a large positive gate bias ($>V_{th}$), on the other hand, slow electron traps are found to additionally affect the slow trapping characteristics.

Experiments P-type (100) Ge wafers were cleaned by de-ionized water, acetone and HF. After this pre-cleaning, oxidation by ECR plasma in Ar and O_2 at 300 ºC under 650 W for 2 s, followed by 1.5-nm-thick Al_2O_3 ALD at 300ºC. PDA was performed for 30 min at 400 ºC in N_2 ambient, followed by 100-nm-thick Au gate electrodes.

Results and Discussions We have proposed a simple and effective method to estimate ΔN_{st} in Ge MOS interfaces [7], here, V_g is repeatedly scanned between V_{start} (V_{max}) and V_{stop} (V_{min}). The density of slow traps responding to C-V scan (ΔN_{st}) can be estimated from the amount of hysteresis (ΔV_{hys}) in the C-V measurement between forward and backward scans, as a function of the maximum effective electric field across gate insulators (E_{ox}). Also, we have found that a large amount of electron slow traps exist in GeO_x and/or close to GeO_x/Ge interfaces. These electron traps are supposed to contribute the C-V hysteresis for not only n-Ge but also p-Ge MOS interfaces. In order to investigate if the electron slow trapping really occurs or not during C-V scans in p-Ge MOS interfaces, the influence of the C-V scan hold time is examined. As shown in Fig. 1, the hold time at the V_{start} points during C-V measurements is varied under constant V_{stop} and V_{start} values. Fig. 2 shows the extracted V_{FB} values in the forward and back C-V scan with changing (a) V_{start} ($V_{start} > V_{th}$) and (b) V_{start} ($V_{start} < V_{th}$) hold time. When the V_{start} ($>V_{th}$) hold time increases, ΔV_{hys} becomes larger. On the other hand, ΔV_{hys} has no change with increasing the V_{start} ($<V_{th}$) hold time. This fact means that electron slow trapping apparently occurs during long-time electrical stress. On the other hand, this electron traps can only be observed und er $V_{start}>V_{th}$ conditions.

Electron slow trapping occurs during forward scan in p-Ge MOS interfaces. Thus, in order to quantitatively evaluate the ΔN_{st} and understand the slow trapping behavior in p-Ge MOS interfaces by using C-V hysteresis, discrimination of the electron and hole slow traps is quite important. Fig. 3(a), (b) show the extracted V_{FB} values in C-V scanned between V_{start} and V_{stop}. Here, V_{FB} in the forward scan keeps increasing with increasing V_{start} under V_{start} larger than V_{th}, meaning that the electron slow trap density can be estimated by increasing electron field under inversion. On the other hand, the hole slow trap density can be estimated by decreasing V_{stop} under constant V_{start} lower than V_{th}. These characteristics allow us to separately evaluate the electron and hole slow trap density in p-Ge MOS interfaces. Fig. 3(c) shows the electron and hole slow trap density in p-Ge MOS interfaces. The electron slow trap density is found to be significantly higher than the hole one, meaning that V_{start} should be carefully determined for slow trap measurement in p-Ge MOS capacitors. Fig. 4 shows the physical images of slow trapping. Here, the time constant of electron trapping into slow traps is widely distributed and traps with very long-time constants exist can near conduction band side, independent of the accumulation condition in n-Ge or the inversion condition in p-Ge MOS capacitors.

Conclusion A new measurement procedure to discriminate hole and electron slow traps has been proposed and applied to Al_2O_3/GeO_x/p-Ge gate stacks. Both electron and hole slow trap densities have been successfully evaluated in p-Ge MOS capacitors The electron slow traps, evident under the strong inversion condition, is very important in understanding the ΔN_{st}-E_{ox} relationship.

Acknowledgement This work was partly supported by the Japan Society for the Promotion of Science (JSPS) KAKENHI under Grant 20K14779 and 17H06148, Casio Science Promotion Foundation and Hirose International Scholarship Foundation, Japan.

References [1] R. Zhang et al., TED (2013) 927 [2] R. Zhang et al., APL 98 (2011) 112902 [3] R. Zhang et al., IEDM (2011), 642 [4] J. Franco et al., IEDM (2013) 397 [5] M. Ke et al., APL (2016) [6] G. Groesenken et al., IEDM (2014) 828 [7] M. Ke et al., IEDM (2018) 791 [8] M. Ke et al., MEE 178 (2017) 132 [9] M. Ke et al., ACS AEM 1 (2019) 311

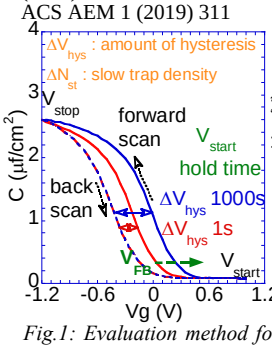

Fig.1: Evaluation method for electron slow trap density by using scan cycle of C-V with different V_{start} hold time.

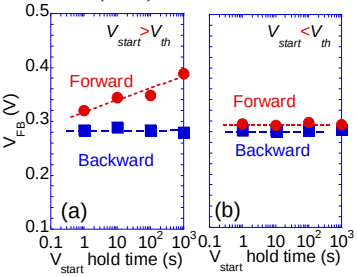

Fig.2: V_{FB} values in forward and back C-V scans with different (a) V_{start} ($V_{start} > V_{th}$) and (b) V_{start} ($V_{start} < V_{th}$) hold time for forward and backward C-V scans with same V_{stop} and V_{start}.

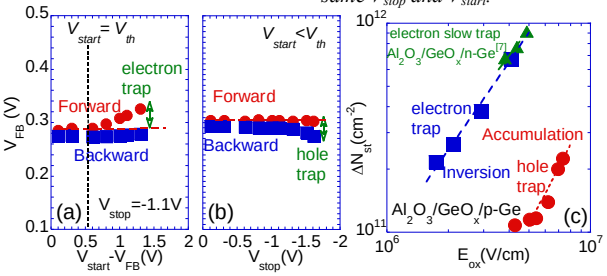

Fig.3: V_{FB} values in forward and back C-V scans with (a) same V_{stop} and increasing V_{start}. (b) same V_{start} and decreasing V_{stop}. (c) hole and electron slow trap density as a function of electron field of across the gate oxide. The electron slow trap density of n-Ge MOS interfaces has also been plotted as a reference [7].

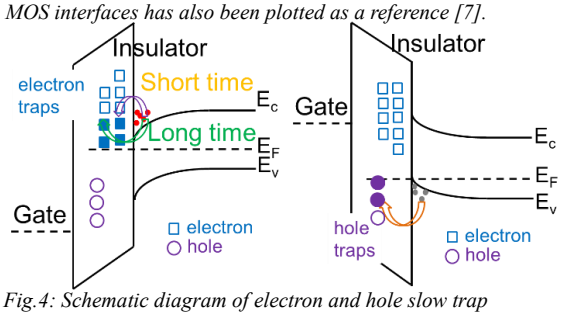

Fig.4: Schematic diagram of electron and hole slow trap responses in Ge p-MOS interfaces.