Simulation Study on the Role of GIDL Current for Erase Operation in FeFETs

IIS, Univ. of Tokyo °(M2)Xiaoran Mei, Fei Mo, Toshiro Hiramoto, and Masaharu Kobayashi

E-mail: meixiaoran@nano.iis.u-tokyo.ac.jp

1. Introduction: FeFET memory, as a kind of state-of-the-art non-volatile memory, has been in the limelight for its small cell size, low-power and high-speed operation since CMOS compatible ferroelectric (FE)-HfO_2 was discovered[1]. Previously, 3D vertical structure has become the mainstream in NAND flash memory, with its characteristics of (1) N-type junctionless transistor and floating-body as 1T memory [2], which accelerates the generation of majority carrier (electron) and (2) GIDL (Gate Induced Drain Leakage) current for fast generation & supply of minority carriers (hole) [3], which enables efficient erase operation (Fig. 1). Therefore, it is natural to consider the same structure and utilize GIDL current for higher performance in FeFET memory. In this work, we investigate the role of GIDL current for erase operation toward 3D vertical FeFET by TCAD simulation, in terms of gate/drain overlap and underlap cases, low/high sweep speed of gate voltage and drain voltage dependence.

2. Simulation Methods: I_d-V_g characteristics of SOI FeFET with both overlap and underlap structure (Fig. 3) are simulated considering 2-D electrostatics, drift-diffusion carrier transport mechanism, and dynamic Preisach model of FE self-consistently [4], with calibrated parameters. The same simulations are also conducted under different sweep speed (DC as 0.1s and fast sweep as 100ns) and drain voltage (50mV, 0.5V and 1V) to observe the different performance of overlap and underlap cases.

3. Result and Discussion: Fig. 4 shows the simulated I_d-V_g curves of gate/drain overlap device at different V_g sweep speed and V_d. Note that displacement current is superimposed and seen at low current level. Overlap device shows MW even at high speed due to hole generation by GIDL. Even with small V_d, gate-drain overlap region causes considerable GIDL current in FeFET. The downtrend of GIDL current as V_g is more negative results from FE switching in this region. Fig. 5 shows the same I_d-V_g curves with underlap device, and GIDL and hole carrier generation do not happen much in erase operation. In this case, MW exists in DC sweep but becomes small in fast sweep. From this comparison, the faster hole carrier generation by GIDL helps to improve the speed of erase operation in FeFET memory applications.

4. Conclusion: In this work, we investigated and revealed the critical role of GIDL current for erase operation toward 3D vertical FeFET by simulations with gate/drain overlap and underlap structure. GIDL current helps to generate the minority carrier in erase operation and then improves the erase speed in FeFET memory.

5. Acknowledgement: This work was supported by JST SICORP (Grant number: 20218786) and JSPS KAKENHI (Grant number: 18H01489).

References

[1] J. Muller et al., VLSI Symp. 2012, pp. 25-26. [2] K. Florent, IEDM 2018, pp. 43-46. [3] Yosuke Komori et al., IEDM.2008, pp. 1-4. [4] C. Jin et al., VLSI Technol., 2019, p. 220–221.

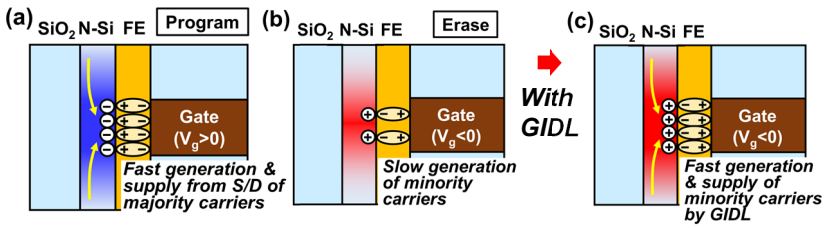


Fig. 1 (a)(b) Schematic of program/erase state of 3D FeFET with N-Si. (c) Erase state with GIDL.

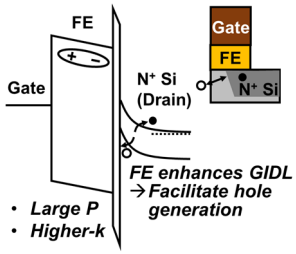
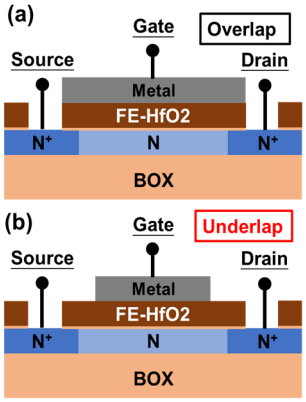


Fig. 2 Band diagram near drain of FeFET.



Default transistor parameters	
N_{sub} [cm^{-3}]	n-type 1×10^{16}
$N_{S/D}$ [cm^{-3}]	n-type 1×10^{20}
EOT_{IL} [nm]	0.5
t_{fe} [nm]	10
L_g [μm]	0.4

Fig. 3. Schematic illustration of SOI FeFET and the default parameter.

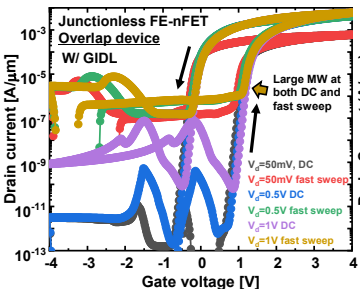


Fig. 4 Simulated I_d-V_g of junctionless FeFET with gate-drain overlap at DC/fast sweep for different V_d.

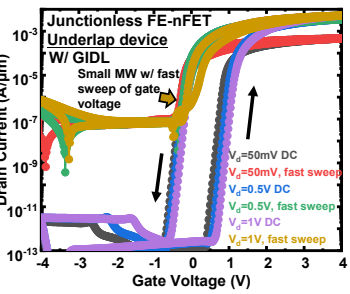


Fig. 5 Simulated I_d-V_g of junctionless FeFET with gate-drain underlap at DC/fast sweep (100ns) for different V_d.