Performance improvement of $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs by ultrathin Y_2O_3 gate stacks with TMA treatment

O T.-E. Lee[1], S.-T. Huang[2], C.-Y. Yang[2], K. Toprasertpong[1], M. Takenaka[1], Y.-J. Lee[2], and S. Takagi[1]
[1]The University of Tokyo, Japan
[2]Taiwan Semiconductor Research Institute, Taiwan
E-mail: leete@mosfet.t.u-tokyo.ac.jp

1. Introduction

The channel mobility and sub-threshold swing (S.S.) of high-k/SiGe MOSFETs are still degraded by high interface trap density (D_{it}) at SiGe MOS interfaces, which is attributable to undesired formation of Ge-O bonds near the interfaces [1]. We have recently reported the superior Si-cap-free SiGe MOS interfacial properties with low D_{it} by a combination of the TiN/6-nm-thick Y_2O_3 gate stacks with TMA treatment and high temperature annealing, attributed to scavenging of GeO_x and healing of weak Ge-O bonds in $SiGeO_x$ interfacial layers (ILs) by Y doping [1-3]. However, the properties of SiGe MOS interfaces with ultrathin Y_2O_3 gate stacks and their FET performance are still not clear. In this work, the electrical characteristics of a $Si_{0.78}Ge_{0.22}$ gate stack with scaled 1.9-nm-thick Y_2O_3 such as D_{it} and leakage current (J_G) are examined. Moreover, $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs with this gate stack are fabricated and the effectiveness of the ultrathin EOT Y_2O_3/SiGe stacks are demonstrated through the electrical characteristics.

2. Experiment

The details of the fabrication process and conditions of the capacitors are described in [3]. Here, the thickness of ALD Y_2O_3 deposition used in this study is 1.9nm. For the fabrication of FinFETs, after gate stack formation, boron ions were implanted with an energy of 10 keV and a dose of $1 \times 10^{15}cm^{-2}$ for S/D formation. Subsequently, activation annealing was performed at 350°C by CO_2 laser. Finally, contacts of the gate, source and drain were formed by Al/Ti.

3. Results and Discussion

The C-V curves and a TEM image of the TiN/1.9nm Y_2O_3 stacks with the TMA treatment are shown in Fig. 1(a) and (b), respectively. The hysteresis-free C-V curves with small hump in the depletion region are found. The CET value is estimated to be 1.43 nm. The thickness of amorphous Y_2O_3 and ILs of the stacks is observed to be 1.7 and 0.5 nm, respectively. Fig. 2(a) and (b) show the energy distributions of D_{it} and J_G as a function of effective E_{OX}, respectively, of the TiN/1.9nm Y_2O_3 stacks with and without the TMA treatment. The lower D_{it} in the stacks with the TMA treatment than that without the treatment is attributable to less amounts of Ge-O bonds at the SiGe interfaces [2,3].

Fig. 3 (a) and (b) summarize S.S. as a function of I_D and g_m/C_{ox} at V_D=-1V as a function of V_G, respectively, of $Si_{0.8}Ge_{0.2}$/SOI and pure SOI p-FinFETs at L_G of 40 nm. The channel fin height of $Si_{0.8}Ge_{0.2}$/SOI and pure SOI FinFETs, fabricated for comparison, is 80/20 nm and 100 nm, respectively. The two types of the gate stacks, Y_2O_3 with the TMA treatment and HfO_2 with the NH_3 treatment, were employed for $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs, while SOI p-FinFETs have HfO_2/SiO_2 stacks as the control samples. These three gate stacks have the same EOT of 1 nm. It is found that S.S. is reduced by 40 % in the $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs by changing the gate stacks from HfO_2 with the NH_3 treatment to Y_2O_3 with the TMA treatment. Moreover, $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs with the Y_2O_3 exhibit 24% and 15% improvement in maximum g_m/C_{ox} against the SOI and $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs with the HfO_2 stacks, respectively. The less trapped charge density can lead to suppression of coulomb scattering as well as the increase in surface carrier concentration at a given V_G, resulting in the improvement of the current drive of the FinFETs with the Y_2O_3/SiGe stacks.

4. Conclusions

The ultrathin TiN/Y_2O_3/SiGe gate stack with CET of 1.43 nm and the low D_{it} of 1×10^{11} $eV^{-1}cm^{-2}$ have been demonstrated by scaling the thickness of Y_2O_3 down to 1.9 nm and the incorporation of Al atoms in ILs through the TMA treatment. The improvement of the performance and reduction of S.S. have been found in the $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs with this gate stack.

Acknowledgements

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References [1] C. H. Lee *et al.*, IEEE IEDM (2013) 40. [2] T.-E. Lee *et al*, Proc. VLSI Symp. (2019) 100. [3] T.-E. Lee *et al*, IEEE Trans. Electron Devices **67** (2020) 4067.

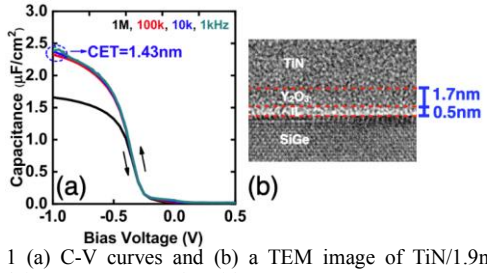

Fig. 1 (a) C-V curves and (b) a TEM image of TiN/1.9nm $Y_2O_3/Si_{0.78}Ge_{0.22}$ gate stacks with TMA treatment.

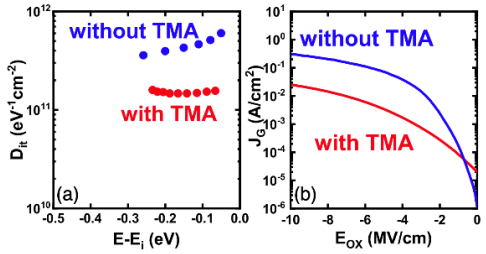

Fig. 2 (a) D_{it} distribution and (b) J_G of TiN/Y_2O_3/SiGe stacks with and without TMA treatment.

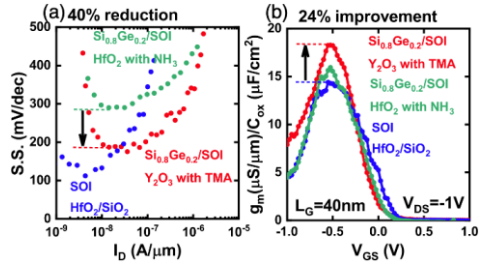

Fig. 3 (a) Sub-threshold swing as a function of I_D (b) g_m/C_{ox} as a function of V_{GS} of $Si_{0.8}Ge_{0.2}$/SOI p-FinFETs and SOI p-FinFETs.