Improvement in FeFET-based Reservoir Computing Capabilities by Using an Inverted Signal Scheme

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1. Introduction We have proposed reservoir computing (RC) [1] by using a new physical reservoir based on FeFETs [2]. However, the computing capabilities are limited due to low currents of FeFETs with gate voltage lower than the threshold voltage [3]. In this study, we propose a new computing scheme employing two FeFETs with the inputs inverted to each other (Fig. 1) to overcome this problem of low I_d under the low gate voltage. Here, the output signals of the two FeFETs are combined and used as the reservoir output nodes. Higher capabilities of RC tasks are demonstrated with the proposed system.

2. Experiment We used two Si FeFETs with the same TiN/$Hf_{0.5}Zr_{0.5}O_2$(10 nm)/SiO_2 (0.7 nm) gate stacks. A randomly generated time-series binary data (u(t)) with 1000 bits and its inverted value sequence ($\bar{u}$(t)) were prepared. The two sequences were transformed to triangular voltage pulses with the center voltage of 1 V and the voltage swing of ±3 V. Here, the bit value '1' and '0' are encoded as positive and negative peak pulses, respectively. The pulse series were applied to each gate of two FeFETs, and each output current I_d of the two FeFETs was uniformly sampled by N points over one pulse width, which are utilized as virtual nodes. The N virtual nodes of each FeFET were combined, providing the total 2N nodes as the reservoir output nodes. Short-term memory (STM) and parity check (PC) tasks were preformed to evaluate RC performance with linear regression to calculate the optimum weight matrix.

3. Results and Discussion STM and PC tasks were performed in three ways: using a single FeFET with original input, another single FeFET with the inverted one and using the two FeFETs. Fig. 2 shows the dependency of the computing capabilities of STM (C_{STM}) and PC (C_{PC}) tasks on the virtual node number from 20 to 400 with the pulse width of 4 μs. It is found that, when comparing at a given node number, C_{STM} and C_{PC} using both original and inverted signals are higher than those using a single signal, irrespective of the node number. The performances gradually increase with an increase in the node number. Fig. 3 shows the squared correlation for STM and PC tasks as a function of T_{delay} when using two FeFETs and a single FeFET with original or inverted input signal. At T_{delay} = 2, the squared correlation is almost 1 in the combination of the original and inverted signals. In addition, higher squared correlation values can also be observed for T_{delay} > 2. Especially for the STM task, slight short-term memory remains until T_{delay} of 8 for the combination of the original and inverted signals, which is much longer than in the original or the inverted signals.

The pulse width dependence of the performance is shown in Fig. 4. The computing capabilities in the combination of the original and inverted signals are higher than in the original or the inverted signals, irrespective of the pulse width. To analyze the origin of this improvement, we separately examined the accuracy of the learning at T_{delay} = 2 for the present data of '1' and '0' separately as a function of the pulse width (Fig. 5). When using a single FeFET, the learning accuracy is much lower for negative pulse ('0' input) than for positive one. This fact indicates that the computing capabilities are mainly limited by the low accuracy under negative pulses. In contrast, when using both the original and inverted signals, the classification accuracy keeps high values regardless of '1' and '0'. This is because, when the single signal is used, I_d under negative pulse, which has lower voltage in most of the time during one pulse term than the threshold voltage of the FeFET, cannot provide enough information for inference, resulting in the lower accuracy [3]. On the other hand, when both the original and inverted signals are used, the input gate voltage of one of the two FeFETs is higher than the threshold voltage, irrespective of positive and negative pulse input, providing high I_d values including sufficient information.

4. Conclusions We have proposed a computing scheme with inverted input signals for improving the computing capabilities in the FeFET-based reservoir computing. It has been demonstrated that the computing capabilities are higher in the combination of the original and inverted signals than in a single FeFET in the conventional scheme.

Acknowledgement This work was supported by JST CREST Grant Number JPMJCR20C3, Japan.

References [1] H. Jaeger, *GMD Report* 148 (2001). [2] E. Nako, et al., *VLSI Symp.*, TN1.6 (2020). [3] Z. Wang, et al., *Si Nanoelectronics Workshop (SNW)* (2021)

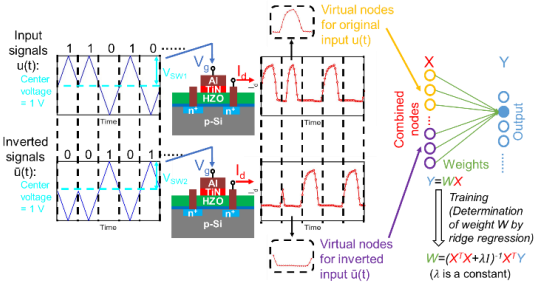

Fig. 1 Proposed reservoir computing scheme utilizing two FeFETs. I_ds from two FeFETs at each period are combined as virtual nodes.

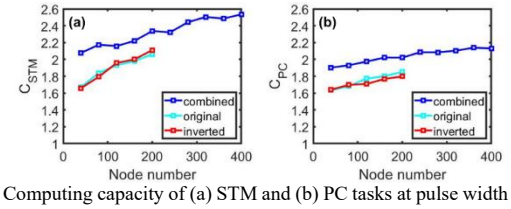

Fig. 2 Computing capacity of (a) STM and (b) PC tasks at pulse width of 4 μs as a function of virtual node number.

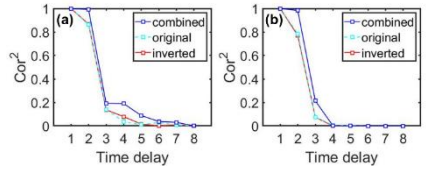

Fig. 3 Correlation values of (a) STM and (b) PC tasks at the pulse width of 4 μs as a function of T_{delay}.

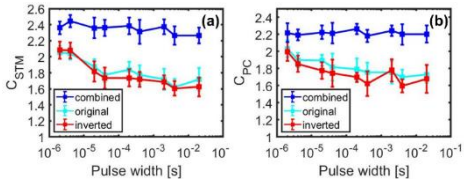

Fig. 4 Computing capacity of (a) STM and (b) PC tasks with changing pulse width.

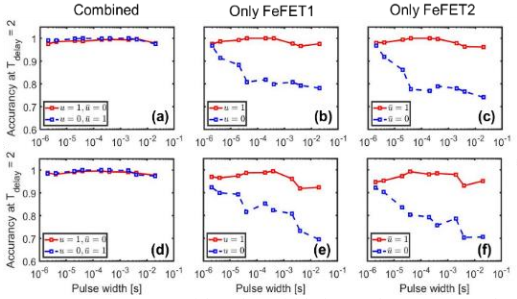

Fig. 5 Accuracy at T_{delay} = 2 with pulse width for (a)(b)(c) STM and (d)(e)(f) PC tasks for different "present" inputs. After combined, the low accuracy under negative pulses is overcome.