応用物理学会学術講演会予稿のタイトル

High-Performance and low-voltage sense-amplifier using GAA-CNTFET with different chirality and channel

°(D)Singh Rohitkumar Shailendra^{1,2}, (M2)Pragya Sharma³, M. Aarthy³, Dr. Hidenori Mimura² ¹Graduate School of Science and Technology, Shizuoka University, Hamamatsu, Japan ²Research Institute of Electronics, Shizuoka University, Japan ³School of Electronics Engineering, VIT, Vellore, India Email: rohitkumar.singh.19@shizuoka.ac.jp, pragyasharma1696@gmail.com

Abstract: This paper is a comprehensive description of GAA-CNTFET based Voltage sense amplifier (VSA) at a 10 nm technology node. Scaling down technology made researchers think about the alternative of traditional silicon transistors, so researchers tend their research towards nanotechnology. Among all the nano-devices CNTFET is a terrific alternative due to its noteworthy properties and manufacturing easiness. CNTFET allows making changes in the channel for fulfilling the global demands of small-sized and ultra-speed. By using the CNTFET's extraordinary properties delay, power and PDP analysis have to be done by taking four different configurations like single chirality single channel (SCSC), single chirality dual channel (SCDC), Dual chirality single channel (DCSC), Dual chirality dual channel (DCDC).

Keywords: Voltage sense amplifier (VSA), Nanotechnology, Chirality, Carbon nanotube field-effect transistor (CNTFET).

CNTFET: Over the past few years traditional silicon transistor comes in its limit sub 10 nm suffers from short channel effects like Drain induced barrier lowering (DIBL), velocity saturation, hot carrier injection, high subthreshold leakage power, random dopant distribution. To overcome these major issues Designer shifted to CNTFET, because of its striking properties like ballistic transport, low V_{th} requirement, high current conduction, and high speed.



Figure (a) shows the circuit diagram of VSA using GAA CNTFET (b) Delay with different chirality (c) Delay with different dielectric material for VSA

Conclusion: Comparative analysis of delay, power, and PDP has been done of VSA by using the four different configurations SCSC, SCDC, DCSC, and DCDC. The result interpretation shows that there is significant trade-off between delay and power consumption. Result shows that better power delay product efficiency for SCDC and DCDC.

Acknowledgment: - We would like to acknowledge Ministry of Education, Culture, Sports, Science and Technology, Japan (MEXT Grant) for the support and Shizuoka University and VIT Vellore for providing necessary facilities for this paper work.