Electrical Characteristics of *n*-Ga_2O_3/*n*-Si Heterojunction Formed by Surface-Activated Bonding

°Zhenwei Wang[1], Daiki Takatsuki[2], Jianbo Liang[2], Naoteru Shigekawa[2], Masataka Higashiwaki[1]

National Institute of Information and Communications Technology[1], Osaka City University[2]

E-mail: Zhenwei.Wang@nict.go.jp

Introduction

Until now, most of semiconductor heterostructures have been fabricated by heteroepitaxial growth. However, its availability is often limited by lattice mismatch between materials. We consider that direct wafer bonding can be an alternative technique to form high-quality heterostructures between materials with large lattice mismatch. In this work, an *n*-Ga_2O_3/*n*-Si heterojunction structure was fabricated by surface-activated bonding (SAB). Test structures were fabricated with the bonded substrate, and their electrical properties were characterized.

Experiments

An unintentionally doped (UID) Ga_2O_3 (001) substrate with an effective electron density (n) of 2.0 × 10^{17} cm^{-3} and an *n*-Si (100)-on-insulator (SOI) substrate with n = 2.0 × 10^{18} cm^{-3} were used in this study. First, the back surface of the *n*-Ga_2O_3 substrate was planarized by lapping and chemical mechanical polishing (CMP). To form good ohmic contacts, the back surface was degenerately doped by Si-ion implantation (box profile: Si = 5 × 10^{19} cm^{-3}, 100-nm thick), followed by implant activation annealing at 800°C. Then, Ti/Au metallization and annealing at 470°C were performed. The *n*-Ga_2O_3 front surface was planarized by CMP and bonded to the *n*-SOI substrate by SAB at room temperature. The bonded Ga_2O_3/Si substrate was processed into a structure with Si pillars on the Ga_2O_3 substrate as shown in Figs. 1(a) and (b), by wet and reactive ion etching processes. Finally, ohmic contacts were formed on the *n*-Si pillars by $Au_{0.99}Sb_{0.01}$ alloy metallization and annealing at 450°C.

Results

All the test structures fabricated on the bonded substrate showed rectifying current density–voltage (*J-V*) output characteristics as shown in Fig. 2, which were attributed to charged defects/traps formed at the bonding interface. A band diagram around the interface is depicted in Fig. 3. It should be noted that a small conduction band offset of 0.05 eV was expected to be formed at the Ga_2O_3/Si interface from the difference of electron affinity (χ) between Ga_2O_3 and Si; however, it was ignored in this study. The built-in potential (qV_{bi}) formed at the interface was extracted to be 0.43 eV from a measured capacitance at thermal equilibrium. The interface charge density was estimated to be 4.4 × 10^{12} cm^{-2} from the qV_{bi}.

Acknowledgement

This work was supported in part by JSPS KAKENHI Grant Number 19H02182.

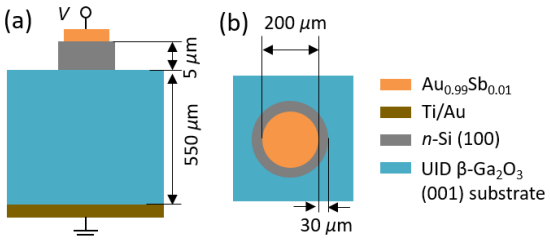

Fig. 1. (a) Schematic cross-section and (b) top view of *n*-Ga_2O_3/*n*-Si heterojunction test structure.

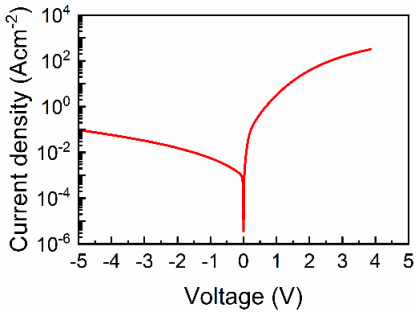

Fig. 2. *J-V* output characteristics of *n*-Ga_2O_3/*n*-Si structure.

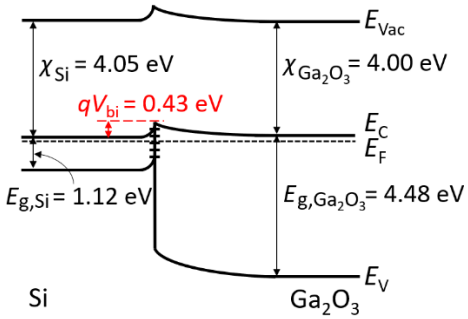

Fig. 3. Band diagram of *n*-Ga_2O_3/*n*-Si heterojunction.