

Application of Millisecond Solid Phase Crystallization of Silicon Films Induced by Micro-Thermal-Plasma-Jet to Bottom-Gate Thin-Film Transistors

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Introduction

Bottom gate thin film transistors (TFTs) fabricated with small grain polycrystalline silicon (poly-Si) film have been attracted much attention because of its advantages⁽¹⁾. However, the conventional methods have some drawbacks such as low mobility as 5~7 cm²/Vs, long thermal cycle, metal contamination. Micro-thermal-plasma jet (μ -TPJ) which can make millisecond solid phase crystallization (SPC)⁽²⁾ of silicon films with good crystallinity, smooth surface and good electrical characteristics is a promised method for making bottom-gate TFTs with good performance.

Experimental

N-type bottom-gate TFTs fabrication diagram is shown in Fig. 1. Electrical characteristics of devices fabricated with different conditions of μ -TPJ are investigated.

Results and discussion

Figure 2 (a) and (b) show transfer characteristics, field electron mobility μ_{FE} and output characteristics of bottom-gate TFT with dimension as length L / width $W = 80/10 \mu\text{m}$. The millisecond SPC film was formed by μ -TPJ under v of 500 mm/s. The millisecond SPC-Si TFTs show high μ_{FE} of 28 cm²/Vs. Figure 3 (a) shows the transfer characteristics of 30 devices fabricated with millisecond SPC film. As shown in Fig. 3 (a), there is small variation among devices. It is the result of small grain size and random orientation of millisecond SPC film. Figure 3 (b) show the $I_d - V_g$ curve of transistor with dimensions as $L/W = 80/20 \mu\text{m}$ when the millisecond SPC formed under different condition of v . The performance of devices becomes worse when v increases. This result suggests millisecond SPC film formed at slow v is a good candidate for small grain bottom-gate TFTs fabrication.

References

- [1]. Z. Xia, L. Lu, J. Li, H.S. Kwok, and M. Wong: IEEE Trans. Electron Devices **65** (2018) 7.
- [2]. H.T.K.Nguyen, H. Hanafusa, Y. Mizukawa, S. Hayashi and S. Higashi, Material Science in Semiconductor Processing **121** (2021) 105357.

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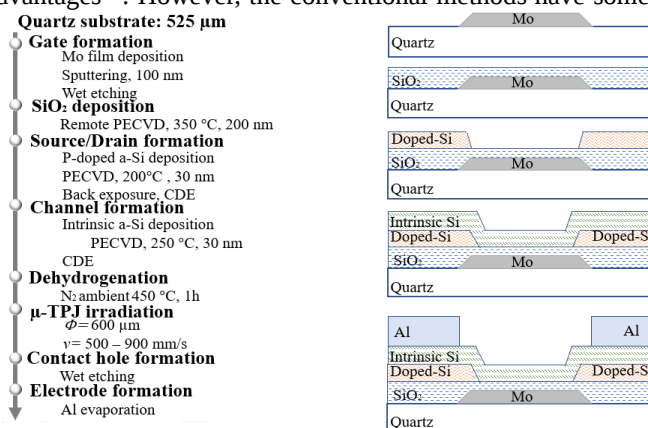


Fig.1. Bottom-gate TFTs fabrication process diagram

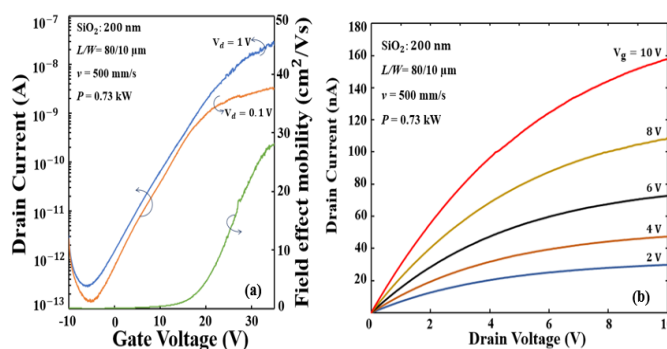


Fig.2. (a) Transfer characteristic, μ_{FE} , (b) output characteristics of TFTs fabricated with millisecond SPC

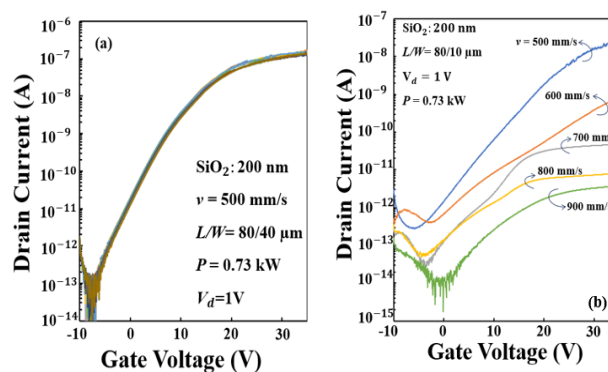


Fig.3. Transfer characteristic of (a) 30 TFTs fabricated with millisecond SPC formed under v as 500 mm/s (b) TFTs fabricated with millisecond SPC formed under different v