Defect control of Y_2O_3-based SiGe MOS interfaces properties

O T.-E. Lee, K. Toprasertpong, M. Takenaka and S. Takagi
The University of Tokyo, Faculty of Engineering
E-mail: leete@mosfet.t.u-tokyo.ac.jp

1. Introduction

SiGe MOSFETs have stirred much attention as p-channel devices, because of the high hole mobility and the appropriate bandgap [1]. However, the undesired formation of GeO_x in the interfacial layers (IL) can be regarded as an origin of the MOS interface degradation [1,2]. As a result, it has been reported that D_{it} can be reduced by a GeO_x-scavenging process, where the choices of atomic layer deposition (ALD) high-k films, metal gate electrodes and annealing temperature are crucial process parameters. In this study, these impacts on D_{it} are systematically examined. Furthermore, the physical origins of the D_{it} reduction in Y_2O_3-based SiGe MOS structures are proposed from the viewpoint of Ge-O networks at SiGe interfaces.

2. Experiment

7-nm-thick non-doped SiGe/p-type Si(100) wafers were cleaned by de-ionized water, acetone and diluted HF. Then, ALD high-k films, including Y_2O_3, Al_2O_3, HfO_2 and ZrO_2, and gate metals, including Al, TiN, Au and W, were employed for gate stack formation. Furthermore, plasma pre-oxidation (PO) [3] and TMA pre-treatments [4] prior to high-k deposition were also studied. PMA was finally performed for stacks at temperature of 300 to 450˚C.

3. Results and Discussion

It is found in Fig. 1(a) that D_{it} of the TiN/Y_2O_3/$Si_{0.62}Ge_{0.38}$ stack with PMA at 300°C is lowest among the Al/Y_2O_3, TiN/Al_2O_3 and Al/Al_2O_3 stacks. Then, the impact of PMA temperature on the TiN/Y_2O_3/$Si_{0.62}Ge_{0.38}$ MOS interfaces were studied. It is found in Fig. 1(b) that D_{it} is minimized at 450ºC for TiN/Y_2O_3, which are also lower than for TiN/Y_2O_3 stacks with PO. Fig. 2 summarizes D_{it} of TiN, W and Au/Y_2O_3/SiGe gate stacks after PMA at 450ºC, and D_{it} of TiN/Y_2O_3/SiGe gate stacks before PMA as a function of Ge contents near interfaces evaluated by EDX. The observed strong correlation between D_{it} and the Ge content near the interfaces after PMA indicates that lower D_{it} in the TiN stacks than those in the W and Au ones is attributable to smaller amounts of Ge-O bonds at the interfaces. On the other hand, significant reduction in D_{it} is observed in TiN/Y_2O_3 stacks after PMA at 450ºC in spite of almost no change in the interface Ge contents, indicating that high temperature PMA itself can also reduce D_{it} of the TiN stacks.

Fig. 3 shows D_{it} of TiN/Y_2O_3, Al_2O_3, HfO_2 and ZrO_2 stacks after PMA at (a) 300 and (b) 450˚C. Here, a large amount of GeO_x is confirmed near the interfaces of the ZrO_2 stacks by XPS analysis. It is found that less GeO_x can lead to lower D_{it} for all the stacks after PMA at 300 and 450˚C, whereas low D_{it} in Y_2O_3 after PMA at 450˚C cannot be explained only by the existence of GeO_x. Thus, this significant reduction in D_{it} can be attributed to a mechanism inherent to Y_2O_3 such as incorporation of Y atoms into networks of Ge oxides and termination of dangling bonds [5].

Fig. 4 shows D_{it} of the TiN/Y_2O_3 stacks and the amounts of Ge-O and Al-O bonds near the interfaces as a function of TMA cycle number in TMA pre-treatment. The existence of the optimum TMA cycle of 10 for reduction in D_{it} can be explained by the two competing effects, less amounts of Ge-O bonds incorporated in the $YSiO_x$-based ILs by TMA and Al-induced increase in D_{it}.

4. Conclusions

We have demonstrated the superior SiGe MOS interfacial properties with low D_{it} by a combination of the TiN/Y_2O_3 gate stacks, PMA and the optimum TMA pre-treatment, attributed to suppression of GeO_x due to scavenging and Y-doping of GeO_x.

Acknowledgements

This work was supported by JST CREST Grant Number JPMJCR1332, Japan and a Grant-in-Aid for Scientific Research (17H06148) from MEXT.

References [1]C.-H. Lee et al., *VLSI Symp.*, 2016, pp. 36. [2]T.-E. Lee et al., *VLSI Symp.*, 2019, T101. [3]T.-E. Lee et al., *J. Appl. Phys.* 127 (2020) 185705 [4]T.-E. Lee et al., *IEEE T-ED* 67 (2020) 4067 [5]L. Zhang et al., *ACS Appl. Mater. Interfaces*, 2016, 8, pp. 19110.

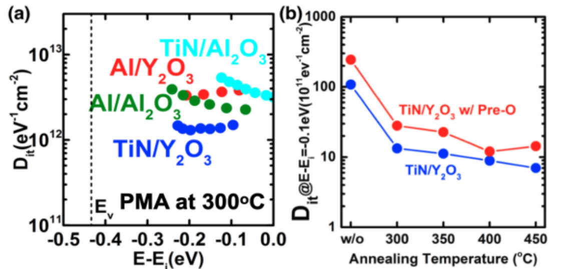

Fig. 1 (a) D_{it} distribution of Al/Y_2O_3, Al/Y_2O_3, TiN/Y_2O_3 and TiN/Al_2O_3 gate stacks after PMA at 300ºC (b) D_{it} as a function of PMA temperature on TiN/Y_2O_3 gate stacks

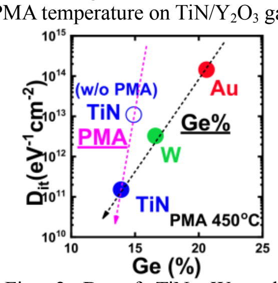

Fig. 2 D_{it} of TiN, W and Au/Y_2O_3 stacks after PMA at 450ºC, and D_{it} of TiN/Y_2O_3 stacks before PMA as a function of Ge% at interfaces

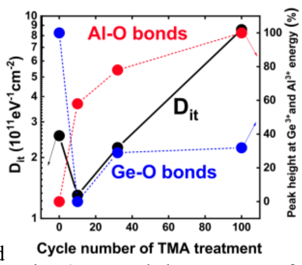

Fig. 4 D_{it}, and the amounts of Ge-O and Al-O bonds near the interfaces as a parameter of TMA cycle number

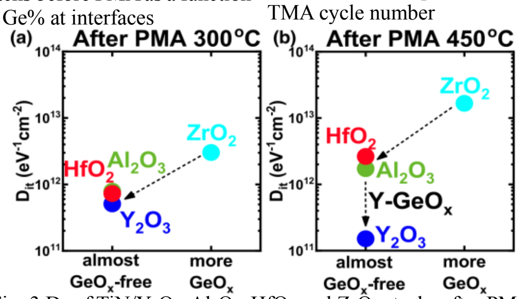

Fig. 3 D_{it} of TiN/Y_2O_3, Al_2O_3, HfO_2 and ZrO_2 stacks after PMA at (a) 300 and (b) 450˚C, and the existence of GeO_x at the interfaces is confirmed by XPS analysis.