Characterization of slow traps in MOS interfaces of TiN/Y_2O_3/SiGe gate stacks

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1. Introduction

One of the critical issues of SiGe MOSFETs, promising as a CMOS channel material, is the formation of high-quality gate stacks. We have demonstrated the SiGe MOS interfacial properties with low interface trap density (D_{it}) over a wide range of Ge contents by using TiN/Y_2O_3 gate stacks with a TMA treatment [1]. However, the slow traps properties in the SiGe MOS interfaces have not been fully studied yet. In this work, we present the impacts of the Ge content of SiGe on the density (ΔN_{st}) and properties of slow traps in TiN/Y_2O_3/SiGe MOS interfaces. Based on the experimental results, the characteristics and a possible origin of the slow traps in SiGe MOS interfaces are discussed.

2. Experiment

TiN/Y_2O_3/SiGe /p-Si MOS capacitors with a TMA pre-treatment and PMA at 450°C were prepared. A simple and effective method to estimate ΔN_{st} from MOS capacitors, shown in Fig. 1, has been proposed for GeO_x-based Ge MOS interfaces [2]. Here, ΔN_{st} was estimated by the amount of the voltage hysteresis between forward and backward C-V sweep as a function of the maximum effective oxide field (E_{ox}), defined by (V_g-V_{FB})/CET, where V_{FB} means the flat band voltage. The cycle measurement with same V_{stop} and increasing V_{start} (Sequence I), was performed for the extraction of electron ΔN_{st} as a function of E_{ox}, whereas the measurements with same V_{start} and increasing V_{stop} was performed for the extraction of hole ΔN_{st}. The measurements with changing the hold time under a given V_{stop} and V_{start} (Sequence II), were performed for the extraction of ΔN_{st} as a function of the hold time, which was varied from 1, 10, 100 and to 999 s. Here, C-V measurements with the different holding time at V_{start} and V_{stop} were performed for the extraction of electron and hole ΔN_{st}, respectively.

3. Results and Discussion

Fig. 2(a) and (b) show ΔN_{st} of $Si_{0.51}Ge_{0.49}$ MOS interfaces for holes and electrons as a function of E_{ox} and V_{start}/V_{stop} hold time, respectively. ΔN_{st} for holes and electrons increases with an increase in the Ge content. The hole and electron ΔN_{st} of GeO_x/Ge MOS interfaces has also been plotted as the reference [2]. The E_{ox} and hold time dependencies are similar between the GeO_x/Ge MOS and Y_2O_3/$Si_{0.51}Ge_{0.49}$ MOS interfaces. Fig. 3 shows the acceleration factor, (a) the slope of log(ΔN_{st})-log(E_{ox}), γ_1, and (b) the slope of log(ΔN_{st})-log(hold time), γ_2, as a function of Ge content of SiGe. The increase in γ_1 with higher Ge contents suggests that higher Ge contents lead to broader energy distributions of defects responsible for trapping near E_c and E_v. On the other hand, the slight increase of γ_2 with higher Ge contents could also be explained by the broader energy distribution, allowing carriers to trap into defect locating at a bit higher energy than E_F through a thermal-activation process [3], illustrated in Fig. 4.

In order to study a possible origin of slow traps, the SiGe MOS interfaces were analyzed by TEM and EDX, revealing the same IL thickness between $Si_{0.78}Ge_{0.22}$, $Si_{0.68}Ge_{0.32}$ and $Si_{0.51}Ge_{0.49}$ MOS interfaces and the higher amount of GeO_x in $AlSiGeO_x$-based ILs with higher Ge contents. Fig. 5 (a) and (b) show the hole and electron ΔN_{st} at E_{ox} of 6MV/cm and at the hold time of 999s, respectively, as a function of the amount of GeO_x in ILs, estimated by XPS. Good correlation between ΔN_{st} and the amount of GeO_x indicates that Ge-O bonds can induce slow traps in ILs, which is suggested by the fact that the inclusion of Ge atoms into SiO_2 networks weakens the network and tends to generate vacancy-related defects [4].

4. Conclusions

Electron and hole ΔN_{st} has been found to increase with higher Ge contents of SiGe. A possible origin of the slow traps in the Y_2O_3/SiGe MOS interfaces is attributable to vacancy-related defects in ILs, whose energy level is close to E_c and E_v, formed by incorporation of Ge-O bonds.

Acknowledgements

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References [1] T.-E. Lee et al., *VLSI Tech.* (2019) 100-101 [2] M. Ke et al., *IEDM* (2018) 791 [3] D. L. Lile et al., *J. Appl. Phys.* 54 (1983) 260 [4] G. Pacchioni et al., *Physical Review B* 56.12 (1997) 7304

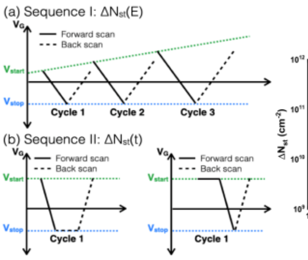

Fig. 1 (a) Cycle measurement with same V_{stop} and increasing V_{start}. (b) Hold time measurement with same V_{stop} and V_{start}. The hold time is varied from 1, 10, 100 and 999s, respectively.

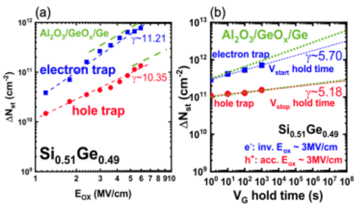

Fig. 2 (a) Hole and electron ΔN_{st} as a function of (a) electron field and (b) V_{start} and V_{stop} hold time of $Si_{0.51}Ge_{0.49}$ MOS interfaces.

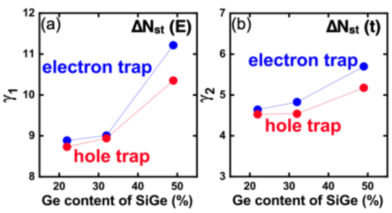

Fig. 3 Acceleration factor (a) γ_1 and (b) γ_2 as a function of Ge content of SiGe.

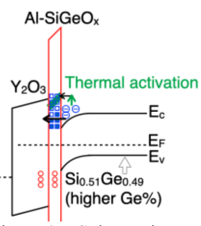

Fig. 4 Schematic diagram of electron slow trap response at $Si_{0.51}Ge_{0.49}$ MOS interfaces.

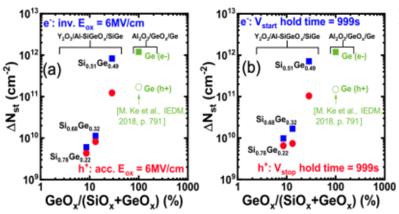

Fig. 5 (a) Hole and electron ΔN_{st} at E_{ox} of 6MV/cm and (b) Hole and electron ΔN_{st} when hold time is 999s as a function of percentage of GeO_x in $SiGeO_x$.