$FeO_y/SrTiO_3$ 界面における 2 次元キャリアガスを用いた電界効果トランジスタ

Field-effect transistor based on two-dimensional carrier gas at the $FeO_y/SrTiO_3$ interface

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$SrTiO_3$ (STO) is fundamentally important for oxide-based electronics since it serves as a standard substrate for a wide range of materials such as high-temperature-superconducting cuprates, colossal magnetoresistive manganites, and multiferroics. Recently, we found that by only depositing a sub-nm-thin Fe layer on top of an STO substrate at room temeprature, it is possible to realize both isolated two dimensional (2D) hole gas (2DHG) and 2D electron gas (2DEG) with ultrahigh mobilities (up to 24000 cm^2/Vs for hole carriers) at $FeO_y/SrTiO_3$ (STO) interfaces [1]. These findings pave a novel way to realize oxide-based devices such as diodes and transistors. Here, as a proof of concept, we demonstrate field-effect transistor (FET) operation using the 2DHG on STO substrates with a back-gate configuration.

As shown in Fig. 1a, the transistor channel was made by depositing a sub-nm-thick Fe film (0.075 – 0.1 nm) on STO substrates in an ultrahigh vacuum chamber. The samples were then patterned into 100×400 μm^2 Hall bars, and FET source and drain electrodes were formed by sputtering a 50 nm-thick Al layer and a lift-off process. We confirmed the existence of a 2DHG with a mobility of 10000 cm^2/Vs (at 2K) in the area below the FeO_y layer. Meanwhile, *n*-type conduction areas are formed under the Al electrode pads because Al induces oxygen vacancies in STO [2]. These mechanisms lead to the formation of a lateral N-P-N junction－the basic structure of an FET－on the STO surface. At low temperatures (~3.5 K), these FET devices exhibit excellent performance, with subthreshold swing values of ~30 mV/dec and on-off ratios of ~10^7 (Fig. 1b). The source-drain $I_{DS} - V_{DS}$ characteristics under a gate voltage exhibit negative differential resistance (not shown), which suggests that the underlying mechanism for this high-performance switching involves a tunneling process at the pn junctions.

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Refs: [1] L. D. Anh *et al.*, Adv. Mater. **32**, 1906003 (2020). [2] T. C. Rödel *et al.*, Adv. Mater. **28**, 1976 (2016).

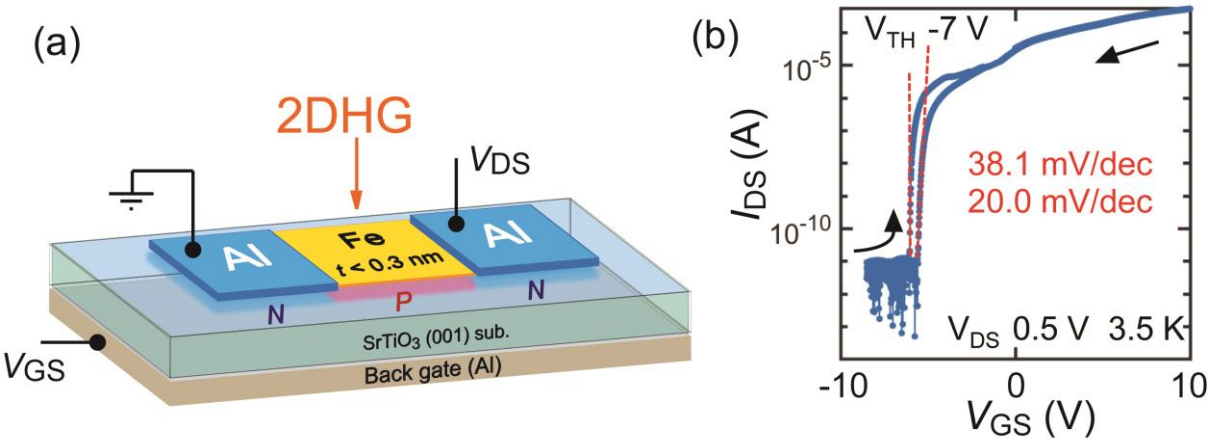

Fig 1. (a) Schematic structure of the back-gate FET device. 2DHG (*p*-type conduction) channel is formed at the STO interface below the FeO_y part, while the *n*-type conduction areas are formed under the Al electrode pads. Gate-source voltage V_{GS} and drain-source voltage V_{DS} are applied as illustrated. (b) I_{DS} - V_{GS} characteristics of the FET device, measured at 3.5 K with a fixed V_{DS} of 0.5 V.