Mobility enhancement of *p*-SnS/*h*-BN heterostructure FET by Ti contact reaction

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1. Introduction

2D materials resistant to short channel effect have enjoyed remarkable achievement in *n*-type FET performance such as reasonable mobility, low subthreshold swing, and high on-current. However, the development of *p*-type counterpart, required for complementary operation, is still in demand owing to intrinsic *n*-type channel by defect-generated electrons and Fermi level pinning to the conduction band. Here, SnS possesses high potential as high-performance *p*-channel < 5 nm other than already well explored WSe_2, because low effective mass is expected due to *s* orbital of Sn for valence band maximum. Recently, PLD grown SnS has been reported to achieve current on/off ratio > 10^6 in 4 nm-thick FET, while the mobility of ~1 $cm^2V^{-1}s^{-1}$ was rather low due to low crystallinity caused by high energy deposition.[1] In this work, SnS was directly grown on top of *h*-BN flakes by thermal PVD to enhance the crystallinity and the device performance of SnS FETs.

2. Results and Discussion

SnS down to 2.4 nm (4 layers) with lateral size of ~1 μm can be obtained on top of mechanically exfoliated *h*-BN substrate by PVD method with pure SnS powder as source and N_2 as carrier gas. Owing to the low tolerance of SnS to oxidation, top-most layer of SnS was usually oxidized. To further explore the effect of surface oxide layer of SnS, SnS/*h*-BN FET with Au contact was analyzed. In the temperature dependent *I*-*V* measurement, the positive shift of threshold voltage (V_{th}) with decreasing temperature was clearly observed, as shown in the inset of **Fig. 2**. This positive shift is not the result of temperature dependence in Fermi-Dirac distribution which will lead to negative V_{th} shift in *p*-FET, but could be ascribed to the temperature dependency of surface doping charge Debye length which is inversely proportional to the square of temperature, as schematically illustrated in **Fig. 1(a)**. This behavior is similar to previous report on InO_x/InSe interface.[2]

To eliminate the doping effect from surface oxide that will hinder the intrinsic performance of SnS *p*-FET, the metal with high oxidation ability, Ti, was introduced as interfacial contact metal. When deposited at ultrahigh vacuum (UHV) condition, Ti could preferentially oxidize by removing the oxygen from the oxide layer on top of SnS, as shown in **Fig. 1(b)**.[3] By reducing surface *n*-doping, SnS FETs with Ti/Au contact are able to exhibit larger V_{th} than one with Au contact and thus, better performance, as shown in **Fig. 2**. Noted that the temperature dependence of V_{th} shift in Ti/Au contact devices becomes opposite.

Finally, by applying Ti/Au contact, the current on/off ratio and mobility of < 5 nm-thick SnS/*h*-BN FETs were improved to the level of thicker devices, as shown in **Figs. 3(a)** and **(b)**. Current on/off ratio more than 10^3 and mobility of ~23.8 $cm^2V^{-1}s^{-1}$ were achieved in 4.2 nm-thick SnS/h-BN *p*-FET. Further progress on these devices such as dual gate structure, is required to increase the on/off ratio to 10^6 for practical application.

References: [1] W. Wang, *et al., Adv. Electron. Mater.* 2019, 1901020. [2] P.-H. Ho, *et al., ACS Nano 2017, 11, 7, 7362.* [3] S. McDonnell, *et al., ACS Appl. Mater. Interfaces* 2016, 8, 8289.

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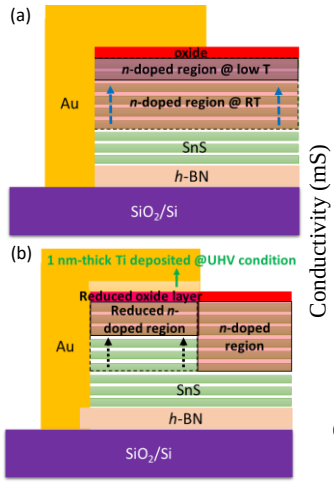

Figure 1. Schematics of (a) temperature-dependent doping range from surface oxide and (b) doping reduction by Ti deposition in UHV.

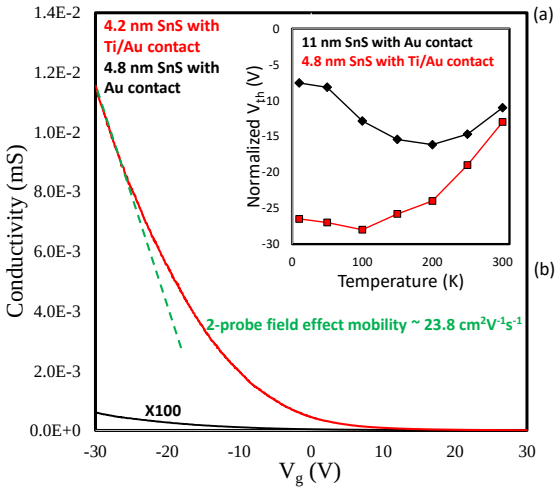

Figure 2. Conductivities of SnS/*h*-BN FET with different contact metals. The inset shows the temperature dependent V_{th} of SnS/*h*-BN FETs.

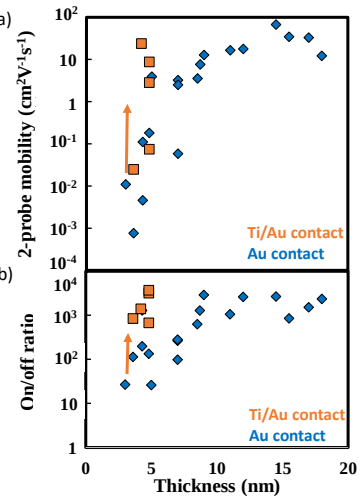

Figure 3. (a) Thickness dependent 2-probe field effect mobility and (b) current on/off ratio of SnS/*h*-BN FETs.