MOS 構造におけるゲート酸化物からの Si-O 延伸モードは界面状態の密度と関係があるか？

Is the Si-O Stretching Mode from Gate Oxide in MOS Structure related to the Density of Interface States?

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To assess the quality of P-channel metal-oxide-semiconductor field effect transistor (p-MOSFET), also called pMOS, two important parameters are often used: the estimation of the density of interface states between the n-type silicon substrate and the silicon oxide layer, i.e. the gate oxide, and also the quality of the silicon oxide layer itself. The importance to reach the lowest density of interface states (D_{it}) is already well established for any semiconductor devices. Here, the optical properties of the silicon oxide are also monitored by Fourier Transform Infra-Red (FTIR) and coupled with the gate oxide process, the chemical cleaning process prior to the gate oxide deposition, and D_{it} measured on pMOS devices.

The pMOS devices are fabricated by Minimal Fab [1,2]: an advanced, cost-effective, semiconductor fab where the area of the required cleanroom level is minimized to the surrounding of the silicon wafers (with a diameter of 12.5 mm), encapsulated in a shuttle during the full fabrication process, thus bypassing the space and budget required for a mega fab [2].

For two pMOS devices A and B realized in a similar process using the same Minimal Fab tools, the D_{it} is estimated by C-V measurements at $5.5\pm1.0 \times10^{10}$ eV^{-1} cm^{-2} and $4.5\pm1.5 \times10^{11}$ eV^{-1} cm^{-2}, respectively. The Si-O stretching mode, located at the wavenumbers from 1000 cm^{-1} to 1250 cm^{-1}, and its deconvolution, is shown in **Fig. 1**. The devices are well deconvoluted into two peaks noted in-phase and out-of-phase (**Fig. 1**) [3,4]. Interestingly, the integrated area of the Si-O stretching out-of-phase is slightly larger for the pMOS device B that also presents a larger D_{it}. This could be attributed to some impurities present at the interface and/or some slight damages due to the fabrication process after the high temperature annealing (1150 °C for 1h) for the gate oxide. The nature of such impurity and its concentration or the possible process damages are still under investigation. Besides, the stoichiometry x of the silicon oxide (SiO_x) can also be determined with the position of the Si-O stretching mode in-phase [3,4]. We estimate a similar stoichiometry about 1.91±0.01 and 1.92±0.01 for the pMOS devices A and B, respectively. Thus, coupling the FTIR analysis with D_{it} could be useful for the determination of the Gate oxide quality and its interface with the Si wafer.

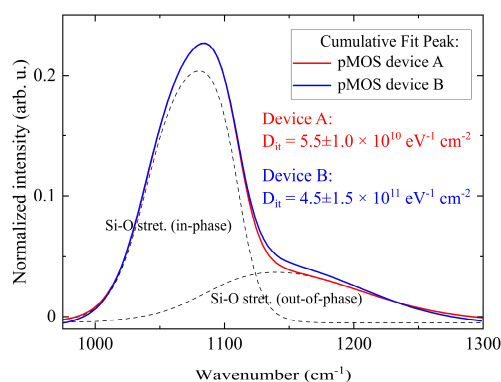

Figure 1: FTIR Si-O stretching mode for two different pMOS devices A and B with respective D_{it}.

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