Design of RV32E RISC-V CPU for Biomedical and IoT Applications

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Introduction

In the quest for the realization of smart societies, there is an increasing demand for sensors and small, low powered yet high performance devices. This is especially prevalent in the fields of biomedical and IoT. How it might work can be seen in Fig. 1, a device operating in pulses of 1-10ms would use the energy from the photovoltaic to power the sensor, process the signals and send the information to the computer.

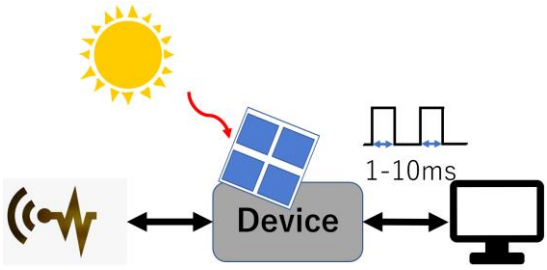

Fig. 1 Proposed optical-powered IoT device workflow

As the devices can be used in various applications, traits such as reprogrammability or versatility would be an attractive trait to have. Towards this end, we would like to propose a RISC-V CPU utilizing RV32E instruction set to be used as a platform for IoT applications. RV32E is similar to the more widely used RV32I instruction set however it contains less registers resulting in a reduction in area size and power consumption. This would allow for the rapid implementation of different ideas and allow for the same chip to be used in different fields as we only need to change the code for each application.

Proposed Architecture

Fig. 2 shows the proposed architecture for the CPU top layer. Unlike many other devices [1-2], our CPU is designed to integrate the necessary storage, RAM and other modules needed to function, allowing for the realization of ultra-small sized devices.

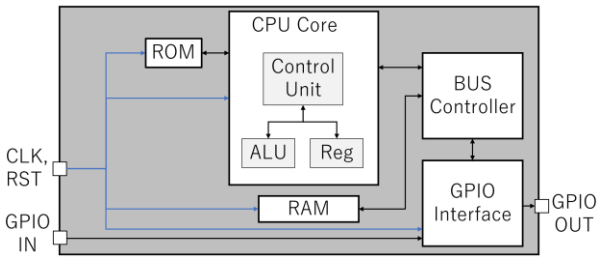

Fig. 2 Proposed CPU top layer architecture for IoT/Biomedical Device

To emulate optical power operation the CPU will be operated using pulse operation with a time period of 1-10ms. In addition, initially the UART protocol will be utilized for communication and programming of the ROM due to its low hardware complexity, and as it is between two devices software addressing is not needed [3].

Results

The CPU top layer is designed using Verilog HDL. The resulting design is then further optimized using Design Vision and ICC compiler, reducing the resulting CPU's area.

Working of an existing design, we reduced the number of registers from 32 registers to 16 registers in addition to several unused states along with the debug pins. As seen in Fig. 3, the removal has resulted in a size reduction from roughly 750 × 750 μm^2 to 690 × 690 μm^2. We are currently working on further reducing the device down further by removing unnecessary modules.

The design is to be implemented using 0.18 μm CMOS process. We plan to manufacture and verify the performance of the chip in the near future.

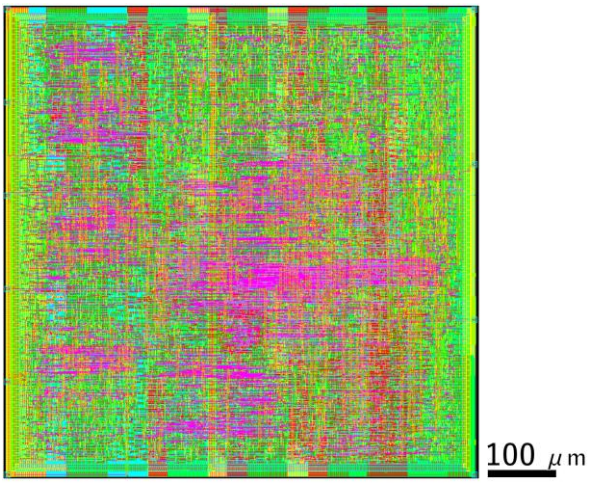

Fig. 3 Resulting layout of CPU chip.

Acknowledgement

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References

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[2] Ronaldo Serrano *et. al.*, ISOCC, 978, 1, 6654, 0174, 6, 21 (2021)
[3] Eric Peña, Mary G. Legaspi, Analog Device, Inc. (2020)