Defect control and enhanced hole gas accumulation of catalyst-free Si/Ge core-shell heterojunction nanowires for HEMT applications

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Nanowires (NWs) are regarded as one of the most promising nanostructures for next-generation high mobility electron transistors (HEMTs), solar cells, and optical sensors due to their outstanding electrical and optical properties. Various types of NWs have been created for potential use in high-performance devices by tailoring their structure and composition, such as axial and radial heterostructures and alloy structures. The p-Si/i-Ge core-shell NWs have been focused on HEMT applications with the design of epitaxial sharp interfaces and type II band alignment [1,2]. In this study, a top-down method of nanoimprint lithography (NIL) together with Bosch etching was investigated for core-shell NW formations to solve catalyst contamination problems and control the vertical alignment of the NWs. Various techniques of chemical etching and thermal annealing were performed to reduce the diameter of core p-SiNWs with minimization of the NW surface defects. The enhanced hole gas accumulation in i-Ge shell region arrays through the Fano resonance effect was observed. The results indicate great potential for realizing future vertical high-speed transistors using Si/Ge core-shell NWs.

P-type SiNW arrays were formed on p-type (100) Si substrates using NIL and a subsequent reactive ion etching (RIE) of Bosch process. The thermal annealing was carried out in Ar, H_2, and O_2 gas atmospheres at 900 ˚C for 10 min. The chemical etching based on hydrofluoric (HF) acid was performed. Then, the optimized thermal oxidation was applied following by etching in HF solution to reduce the diameter of the p-SiNWs from 200 nm to 50 nm. The intrinsic Ge (i-Ge) shell layers were formed by chemical vapor deposition using a 10-sccm GeH_4 at 500 ˚C. The total pressure was set at 8 Torr with N_2 gas mixing and the 60-sec shell growth time.

The ESR signals of defects observed from p-Si NWs with various thermal annealing are presented in Fig. 1. The relationship between each thermal annealing, thermal oxidation followed by HF etching, and after p-Si/i-Ge core-shell NW formation is summarized in Fig. 2. Thermal annealing after NW formation is effective for removing defects and

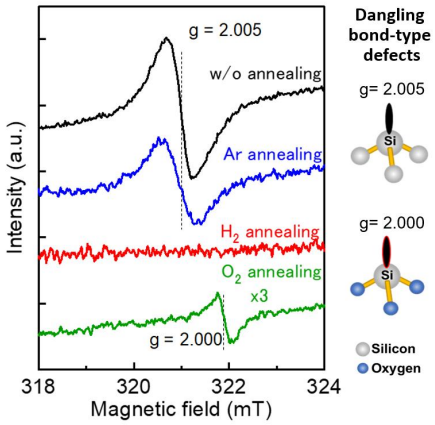

Fig. 1 ESR signals before and after annealing in an Ar, H_2 and O_2 gas atmosphere, and the defect models with g-value of 2.005 and 2.000.

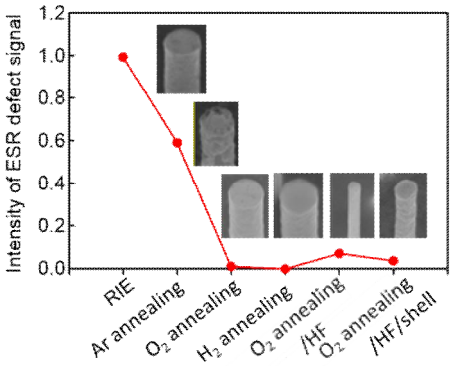

Fig. 2 Dependence of ESR defect intensity and SEM images observed in p-SiNWs with various thermal annealing, and p-Si/i-Ge core-shell NWs.

repairing the crystallinity of the p-SiNW surfaces. The type of annealing atmosphere strongly influences the surface morphology of the NWs. Aggregation of defects proceeds on the p-SiNW surface by annealing in an Ar gas atmosphere; ultimately the defects form voids, markedly increasing the roughness. Annealing in O_2 and H_2 gas atmosphere keeps the p-SiNW surfaces smooth and defects disappear. The combined method of thermal oxidation and chemical etching is thus a very effective process that simultaneously achieves the removal of the surface damaged layer of p-SiNWs and reduction of the NW diameter. The influence of defects at the p-Si/i-Ge core-shell NW interface on the hole gas accumulation effect will be discussed on-site.

[1] N. Fukata, et al., ACS Nano. 9 [12] (2015) 12182-12188.
[2] X. Zhang, et al., ACS Nano. 13 [11] (2019) 13403-13412.