Characterization of Interface Traps Near Valence Band by Split *C-V* measurement

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SiC is one of the most promising wide-bandgap semiconductors for power devices. However, the high density of interface states (D_{it}) in 4H-SiC/SiO_2 structures leads to the poor properties of 4H-SiC MOSFETs [1]. There are several methods to extract D_{it}, like simultaneous high-low *C–V* technique and conductance method. But the D_{it} near valence band (E_V) of P-channel MOSFETs cannot be extracted by these methods.

In this work, the split *C–V* technique was applied on P-channel 4H-SiC MOSFETs to acquire gate-channel capacitance–gate voltage (C_{gc}–V_g) curve for investigation of D_{it} near E_V in 4H-SiC/SiO_2 structures, though this technique is adapted to mobility evaluation since 1982 [2].

P-channel lateral MOSFETs were fabricated on a (0001) Si-face 4H-SiC n-type epitaxial layer (1×10^{16} cm^{-3}). A 50 nm thick gate oxide was formed by dry oxidation at 1200 °C. The samples were treated with NO at 1250 °C for 10 and 30 min (denoted as NO-10 and NO-30). N^+-poly Si was deposited as gate electrode. Channel length of 10μm was used. C_{gc}–V_g curves were measured with the split *C–V* measurement configuration shown in the inset of Fig. 1. All the measurements were performed at room temperature.

To extract the D_{it} near E_V, it is necessary to exclude the AC and DC signals response of interface traps in the split *C–V* measurement. The increased frequency of split *C–V* measurement can eliminate the capacitance (C_{it}) caused by response of interface traps to AC signals [3].

In split *C–V* measurement, the gate voltage was scanned from the inversion region to the depletion region to suppress the variation of the measurements caused by the shift of the threshold voltage.

The method to eliminate the stretch-out effect caused by response of interface traps to DC signals is shown in Fig. 1, where an ideal C_{gc}–V_g curve and a measured C_{gc}–V_g curve at a high frequency of 100 kHz are shown [3]. First, the same C_{gc} values are found on the ideal and measured C_{gc}–V_g curves, and the shadow area is the result of integration of ideal C_{gc}–V_g curve. Shadow area in Fig. 1 is the surface charge in inversion channel (shown as qN_{free}). N_{free} is the free hole density in inversion channel.

Then，the split *C–V* measurement was performed on the same sample at a low frequency of 1 Hz. N_{total} which is the total hole density can be extracted by integration of the 1 Hz C_{gc}–V_g curve. One of the advantages of using the split *C–V* technique is that the errors derived from the assumption of the threshold voltage can be excluded.

The trapped hole density (N_{trap}) is obtained by subtracting N_{free} from N_{total}, as follows:

$$N_{trap}(V_g) = N_{total}(V_g) - N_{free}(V_g) \quad (1)$$

From this function, D_{it} near the E_V is calculated.

In Fig. 2, D_{it} near E_V is shown according to this method. The D_{it} value is around 10^{12} cm^{-2} eV^{-1} near E_V. Compared to the D_{it} values of the NO-10 sample, the D_{it} values of NO-30 sample are reduced by 80% at $E - E_V = 0.08$ eV. This result shows similarity with D_{it} near E_C of N-channel 4H-SiC MOSFETs [4]. According to [5], there is no clear difference in mobility of NO-10 and NO-30 sample ($\mu_{eff} \approx 17 cm^2/Vs$). This shows the mobility is not strongly influenced by D_{it} near E_V.

From these results, it is concluded that this new characterization method can be adapted to calculate D_{it} near E_V for P-channel 4H-SiC MOSFETs. The nitridation process can reduce D_{it} near E_V, but it is unable to completely eliminate the traps. The interface traps near E_V do not play a fatal role in mobility deterioration for P-channel 4H-SiC MOSFETs.

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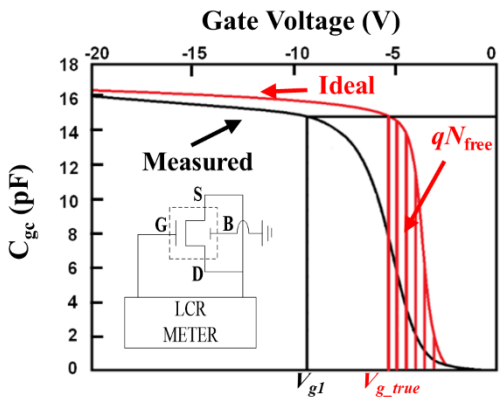

Fig. 1. Illustration of Procedure for extracting free hole density

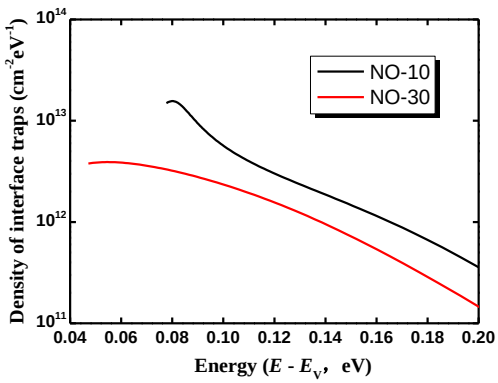

Fig. 2. D_{it} near E_V