Reduction of I_d-V_g hysteresis in SiO_2/MoS_2 n-FET by insertion of h-BN interfacial layer

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1. Introduction Molybdenum disulfide (MoS_2) has become more and more attracting as a next generation two-dimensional (2D) MOSFET channel material because of the suitable bandgap of ~1.1–2 eV for CMOS, and possible suppresses the short channel effect than silicon [1]. However, the reliability issues have not been studied clearly. Recently, annealing can effectively impact the interface properties and reduce the density of border trap which have been reported [2]. On the other hand, the reduction in I_d-V_g hysteresis is still strongly needed. Hexagonal boron nitride (h-BN) has attracted widespread attention due to its special capabilities such as electric insulation and chemical stability[3]. In this study, in order to reduce the I_d-V_g hysteresis, we investigate the effect of inserting h-BN interfacial layer in MoS_2 n-FET with MoS_2/SiO_2/p^{++} Si gate stacks.

2. Experiment Process flow and device structure are shown in Fig.1. Firstly, we cleaned the 300-nm-thick SiO_2-coated p^{++}-Si substrates by 20 min sonic and 30 sec O_2 plasma. After pre-cleaning, h-BN crystals were exfoliated with a tape on the SiO_2/p^{++}-Si substrates. Then we placed the MoS_2 crystals exfoliated with a blue tape on h-BN/SiO_2/p^{++}-Si substrates via a dry transfer process by using polycarbonate film at 180°C. 10-nm-thick Ti and 40-nm-thick Au electrodes were fabricated using electron beam lithography and electron beam metal deposition, followed by 1.5 h annealing in vacuum at 250°C.

3. Results and Discussion Fig.2 shows the I_d-V_g characteristics in 300-nm-thick SiO_2/MoS_2 n-FET w/ and w/o annealing. It is observed that improvement to hysteresis of I_d-V_g curves by annealing, and the hysteresis is reduced from 59 to 17 V. Next, I_d-V_g characteristics in 300-nm-thick SiO_2/tri-layer MoS_2 n-FET with varied minimum gate voltage from -40 V to -10 V are shown in Fig.3. The repeated scan with different minimum gate voltage leading to a changed I_d-V_g hysteresis. Where minimum gate voltage is decreased down to -20 V, forward I_d-V_g starts to shift toward negative voltage. In Fig.4, we compare I_d-V_g characteristics in 300-nm-thick SiO_2/MoS_2 n-FET w/ and w/o insertion of h-BN interfacial layer. It is observed that hysteresis is significantly reduced from 17 to 4 V, proving the effectiveness of inserting h-BN interfacial layer to decrease hysteresis of MoS_2 n-FET. Finally, we summary the hysteresis of MoS_2 n-FETs in this work. After we induce annealing process and insertion h-BN interfacial layer, the hysteresis is reduced to 29% and 23%, respectively.

4. Conclusions We have investigated 300-nm-thick SiO_2/(h-BN)/MoS_2 n-FETs. And we have found the impact of annealing process and inserting h-BN interfacial layer on hysteresis reduction in SiO_2/MoS_2 n-FETs.

Reference

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[2] Z. Ping, et al., ACS Appl. Electron. Mater. **1** (2019), 1372-1377.
[3] M. J. Molaei, et al., ACS Appl. Electron. Mater. **3** (2021), 5165-5187.

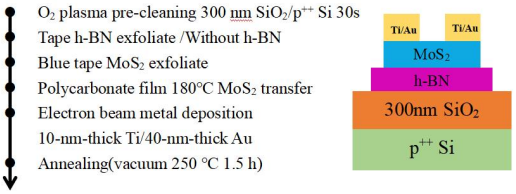

Fig.1 Process flow and device structure of 300-nm-thick SiO_2/h-BN/MoS_2 n-FET

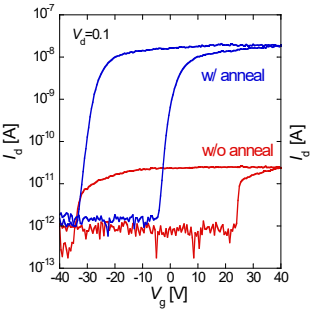

Fig.2 I_d-V_g characteristics in 300-nm-thick SiO_2/MoS_2 n-FET w/ and w/o annealing.

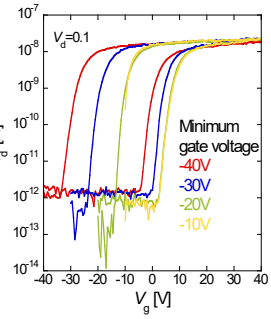

Fig.3 I_d-V_g characteristics in 300-nm-thick SiO_2/MoS_2 n-FET with different minimum gate voltage.

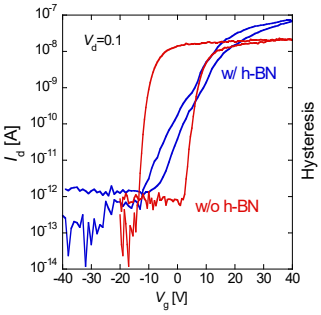

Fig.4 I_d-V_g characteristics in 300-nm-thick SiO_2/MoS_2 n-FET w/ and w/o insertion of h-BN interfacial layer.

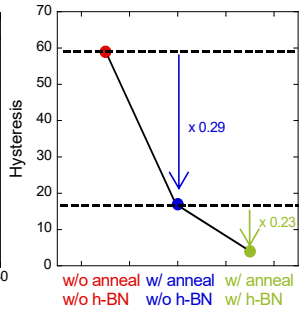

Fig.5 Hysteresis of MoS_2 n-FET w/o anneal and w/o h-BN, w/ anneal and w/o h-BN, w/ anneal and w/ h-BN.