

Subthreshold characteristics of 4H-SiC n- and p-channel MOSFETs at low temperature

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Extremely high density of interface states (D_{it}) exist in SiC MOS systems and the D_{it} values rapidly increase with approaching the conduction band edge (E_C) and the valence band edge (E_V) [1]. However, conventional characterization methods of D_{it} based on C - V measurement of MOS capacitors have limits to estimate D_{it} at the energy level very close to the band edges (e.g., $E_C - E_T < 0.2$ eV). In previous studies, D_{it} very close to E_C was evaluated from subthreshold slopes of MOSFETs at low temperature [2, 3]. On the other hand, very few studies have been reported on the D_{it} very close to E_V and no comparison with the conventional characterization methods has been made. In this study, D_{it} very close to both E_C and E_V was evaluated from the low-temperature subthreshold slopes of n- and p-channel MOSFETs annealed in NO or N₂.

The lateral n- and p-channel MOSFETs were fabricated on p- and n-type 4H-SiC (0001) epilayers on p- and n-type substrates, respectively. The doping concentrations of the p- and n-type epilayers were $1 \times 10^{15} \text{ cm}^{-3}$ and $8 \times 10^{15} \text{ cm}^{-3}$, respectively. The gate oxide was formed by dry oxidation at 1300 °C for 20 min, followed by NO annealing (1250 °C, 70 min) or N₂ annealing (1400 °C, 45 min) [4]. The oxide thickness was about 30 nm, and the channel length and width were 8–10 μm and 170 μm , respectively. Gate characteristics of the fabricated MOSFETs were measured at 77, 100, 200 and 300 K.

Fig. 1 shows the subthreshold characteristics of the fabricated n- and p-channel MOSFETs at 77, 200, and 300 K. In order to estimate D_{it} very close to the band edges, the SS values at the normalized drain current ($I_{DN} = I_D \times L/W$) of 1×10^{-10} A (n-channel) and 1×10^{-11} A (p-channel) at different temperatures were used. For estimating the energy levels of D_{it} , the theoretical drain current was calculated using the following approximation formula:

$$I_{DN} = en_{\text{free}}(E_f)\mu V_d \quad (1)$$

where e is the elementary charge, $n_{\text{free}}(E_f)$ is the density of free carriers, μ is the mobility of free carriers, and V_d is the drain voltage. In the calculation, the mobilities of electrons and holes were assumed to be constant and the two-dimensional density of states was considered for the calculation of n_{free} . Fig. 2 depicts comparison of the D_{it} distributions obtained from the SS values in this study and extracted by the C - ψ_s method from C - V characteristics of SiC MOS capacitors in our previous study [4]. D_{it} in the energy range very close to the band edges ($E_C - E_T < 0.2$ eV or $E_T - E_V < 0.2$ eV) was obtained. The extracted D_{it} values show good agreement with the results of C - ψ_s method in the assessable energy range of the C - ψ_s method and it follows the trends extrapolated from the C - ψ_s results in the energy range closer to the band edges. The N₂-annealed p-channel MOSFETs exhibited a slightly lower D_{it} than the NO-annealed ones at the energy levels very close to E_V , and the peak value of field-effect mobility (μ_{FE}) of the N₂-annealed p-channel MOSFETs (17 cm²/Vs) was higher than that in the NO-annealed ones (13 cm²/Vs) at 300 K [4]. On the other hand, although the NO-annealed n-channel MOSFETs showed a slightly higher D_{it} at the energy levels very close to E_C than the N₂-annealed ones, the peak value of μ_{FE} in the NO-annealed n-channel MOSFETs (40 cm²/Vs) was higher than that in the N₂-annealed ones (34 cm²/Vs) at 300 K [4].

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[3] T. Kobayashi *et al*, *Appl. Phys. Lett.* **108**, 152108 (2016). [4] K. Tachiki and T. Kimoto, *IEEE Trans. Electron Devices* **68**, 638 (2021).

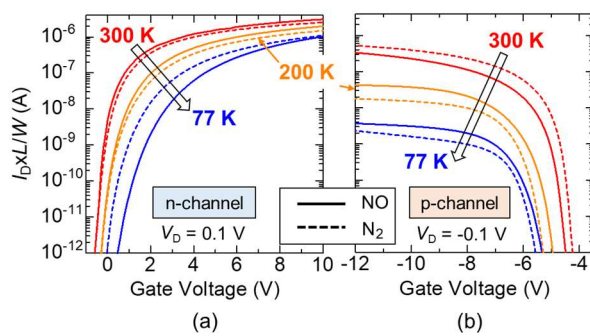


Fig. 1. Subthreshold characteristics of NO- and N₂-annealed (a) n-channel and (b) p-channel SiC (0001) MOSFETs at different temperatures (77, 200 and 300 K).

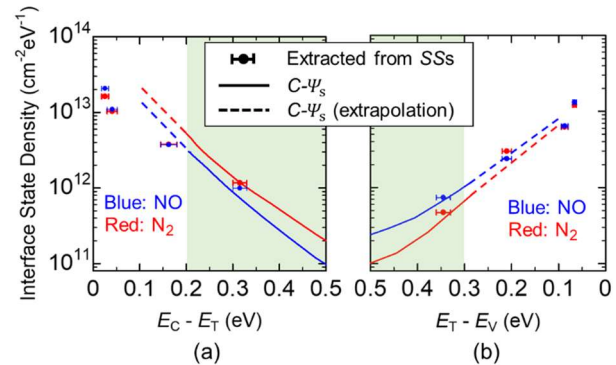


Fig. 2. Comparison of D_{it} distributions extracted by the C - ψ_s method from MOS capacitors and extracted from SSs of SiC MOSFETs at different temperatures near (a) E_C and (b) E_V .