3D NAND Memory Operation of Oxide-Semiconductor Channel FeFETs

IIS, Univ. of Tokyo [1], d.lab, Univ. of Tokyo [2], °(M2) Junxiang Hao[1], (D1) Xiaoran Mei[1], Takuya Saraya[1], Toshiro Hiramoto[1], and Masaharu Kobayashi[1,2]

E-mail: jx-hao@nano.iis.u-tokyo.ac.jp

Introduction

Since the discovery of ferroelectric HfO_2 (FE-HfO_2) in 2011 [1], FeFET has attracted great interests worldwide due to its advantages such as CMOS process compatibility and low power consumption. For higher integration density, poly-Si channel 3D vertical FeFETs have been reported [2]. However, challenges of high write voltage, reliability and low-channel mobility remain. To overcome those challenges, vertical oxide semiconductor (OS) channel FeFETs are demonstrated [3]. For realizing array operation, the characteristic of FeFETs NAND-string needs to be studied but not fully understood yet [4-5].

In this paper, key challenges in 3D NAND OS channel FeFETs such as (1) pass voltage disturb (2) write interference from adjacent wordline and (3) inhibit operation are studied by TCAD simulation.

Simulation methods, results and discussion

A. Simulation method: 5-transistors model, which consists of 3 FeFETs and 2 selectors has been built in TCAD simulator. Fig. 1 shows the model structure and parameters. The charcteristic of T2 is focused when operation voltages are applied to all transistors. DC voltages are used and only static FE properties are considered. In write operation, 5V gate voltage is appiled to wordlines (WLs) to intialize all cells into ERS state with low V_{th}, which corresponds to block erase in NAND Flash. Negative voltages are used for writing the target cells into PRG state with high V_{th}. 0.3V bitline (BL) voltage is used for read out. The sensing ability is evaluted by memory window (MW) and current ratio, which are defined as V_{th} difference when drain current is 100nA and the current ratio between ERS state and PRG state when gate voltage of target cell is 0V, respectively.

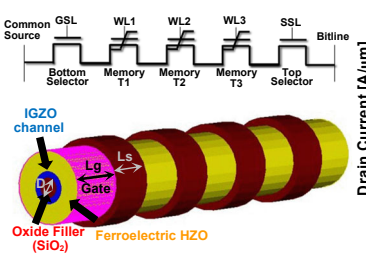
B. Pass voltage disturb: Positive pass voltage (V_{pass}) is necessary to drive unselected cells in a NAND type array, while it may flip the polarization and disturb the PRG state of written cells. After initialized to ERS state, the selected cell T2 is PRG by -5V and returns to the V_{pass}, then PRG state with V_{pass} disturb is read out. The I_d-V_g curves under different V_{pass} disturb are showed in Fig .2(a). PRG states shift more with larger pass voltages. Current ratio in the worst sensing scenario (T1 and T3 are in high V_{th} state) is also extracted under different V_{pass} (Fig .2(b)). V_{pass} has an optimal range for high sensing ability, while larger V_{pass} is desired for larger read current, which is related to read speed. Therefore, 1.0V V_{pass} can be chosen to take balance.

C. Interference from neighbor WL: The interference from neighbor WL may disturb the written cell, espcially when the device size is scaled down. In this part, adjacent memory cells are programmed. Fig. 3(a) shows the I_d-V_g curves of PRG and ERS state of T2, after writing T3. The PRG state V_{th} of T2 is shifted left obviously, indicating the state is interfered by the writing process of the neighbor WL. Polarization charge distribution has been extracted before writing T3 and after writing T3 in Fig. 3(b). The polarization at drain side of T2 is partially flipped after writing T3 due to the electrostatic coupling between the WLs. The interference can be suppressed by using smaller write voltages, but larger write voltage (5V) can be selected for larger MW.

D. Inhibit mode: In 3D NAND array, inhibit mode is necessary for write operation. We studied the conventional inhibit method, in which the potential from BL propagates to the target cell. The GSL is closed firstly, then larger voltages are appiled on BL. The write voltage is applied on the target cell, while V_{pass} is applied to unselected cells. The target cell is read out after inhibit operation. Fig. 4(a) shows the I_d-V_g curves after inhibit operation. The MW is kept well while BL voltage is negatively stronger than -3V as shown in Fig. 4(b).

E. Summary: In this paper, the feasibility of vertical OS FeFETs on NAND type application is studied and operation voltages can be opitimized to satisfy the requirement from disturb, interference and inhibit mode.

Reference: [1] J. Müller et al., IEDM 2013 [2] K. Florent et al., VLSI Symp 2017 [3] Z. Li et al., EDL 2022 [4] M. Pešić et al., IEDM 2021 [5] Gihun Choe et al., TED 2021



Name	Value
Gate Length (Lg)	30 nm
Spacer Length (Ls)	20 nm
Oxide filler Diameter (D)	10 nm
IGZO channel Thickness	3 nm
FE layer Thickness	10 nm
Carrier Concentration	$1\times10^{19}/cm^3$
Saturation Polarization	$23\mu C/cm^2$
Remnant Polarization	$20.1\mu C/cm^2$
Coercive Field	1.16MV/cm

Fig. 1: 5-Tr model schematic and structure simulation device parameters in this paper.

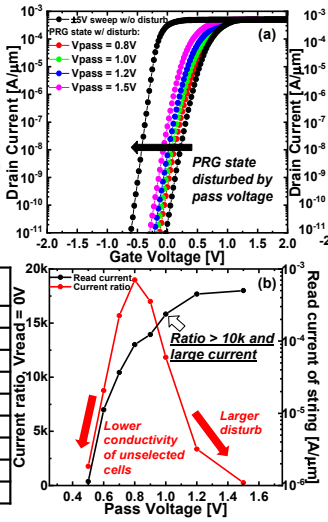


Fig. 2: (a) Simulated I_d-V_g curves at different V_{pass} (b) Extracted current ratio and read current VS V_{pass}.

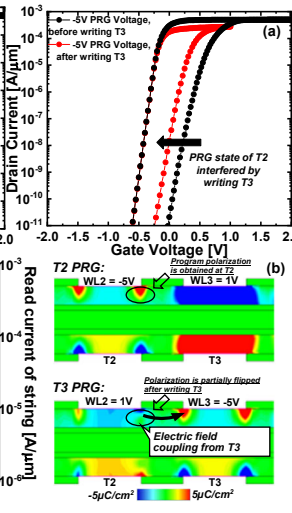


Fig. 3: (a) Simulated I_d-V_g curves of T2. (b) Polarization charge before/after writing T3.

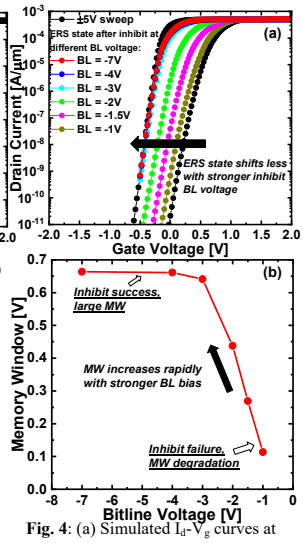


Fig. 4: (a) Simulated I_d-V_g curves at different inhibit BL voltages. (b) Extracted MW after inhibit operation.