A Simulation Study on Memory Characteristics of Oxide-Semiconductor Channel Antiferroelectric FETs Using Half-Loop Hysteresis

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Introduction: HfO_2-based ferroelectric FET memories have attracted much attention due to its CMOS capability and potential low power consumption [1]. Particularly, oxide semiconductor (OS) such as IGZO channel based FeFETs have been recently demonstrated and show great potential because of its high mobility and no low-k interfacial layer formation in 3D structures [2]. However, OS is typically n-type channel material which hardly generates minority hole carriers, causing the weak erase issue in OS channel FeFETs. Previously, antiferroelectric FETs (AFeFETs) have been proposed for efficient erase operation with OS channel by using half-loop hysteresis [3]. But the memory characteristics of OS channel AFeFETs have not been fully discussed yet.

In this work, we developed a compact AFeFET model, studied the memory characteristics of OS channel AFeFETs by varying design parameters, and provided design guide for potential memory applications.

Methods: The device structure and simulation framework are shown in Fig. 1. An AFeFET is modeled by a series connection of a junctionless FET [4] and an AFe capacitor. To describe the charge-voltage relationship of AFe layer, an AFe Preisach model is firstly developed by using the turning point method. The voltage division and charge density in the transistor and AFe capacitor are determined by self-consistently solving analytical equations of the AFE Preisach model and junctionless FET model. To calculate the drain current, the Newton method has been used to solve Poisson equation along the channel direction. Mobile charge and drift-diffusion current have been calculated at each bias voltage.

Results and discussions: First, we fabricated and measured 10 nm-thick HZO-based AFe capacitors with Zr concentrations [Zr] of 70, 80, 90%. Next, the AFe Preisach model fit to the measured data and the parameters were calibrated. As shown in Fig. 2, the historical trajectory was well reproduced by the calibrated model for the arbitrary V_{AFe} wave forms. Then, we simulated AFeFET characteristics with the calibrated AFe parameters by varying device parameters. Here, we focus on discussing the results of the most sensitive device parameters: AFe thickness (t_{AFe}) and [Zr]. In Fig. 3(a), I_{on}/I_{off} largely increases by increasing t_{AFe}. From the operation point analysis, while the load line is fixed, half-loop hysteresis curves have been largely shifted because of the paraelectric capacitance (Fig. 3(b)). As t_{AFe} increases, paraelectric capacitance decreases and thus the operation points shift downward. The erase operation point moves closer to subthreshold region and I_{off} is reduced. In Fig. 4(a), I_{on}/I_{off} largely increases by decreasing [Zr] and becomes larger than 10. Note that as half-loop hysteresis shifts to the left for low [Zr], V_{FB} is adjusted to obtain appropriate operation points at retention state. As shown in Fig. 4(b), lower [Zr] HZO shifts the erase operation point closer to subthreshold region and thus I_{off} is reduced.

Summary: We developed the simulation framework and investigated the memory characteristics of OS channel AFeFET using half-loop hysteresis with the calibrated AFe Preisach model. This work demonstrated the potential of OS channel AFeFETs for memory applications.

References: [1] J. Muller et al., VLSI Symposium 2012, pp. 25-26 (2012). [2] F. Mo et al., VLSI Symposium 2019, pp. 42-43 (2019). [3] Zhuo Li et al., IEEE SNW., pp. 9–10 (2022). [4] B. -W. Hwang et al., IEEE TED, vol. 62, no. 1, pp. 171-177 (2015).

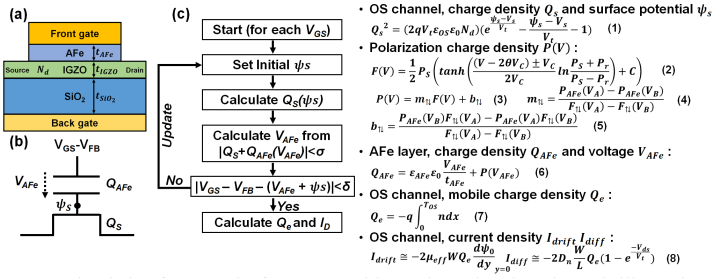

Fig. 1 Simulation framework of AFeFETs with OS channel. (a-b) Schematic illustration of simulated device structure, (c) modeling and simulation flow chart, and equations.

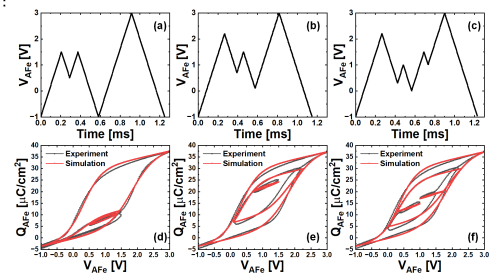

Fig. 2 Measured and simulated minor loop & historical trajectory (d-f) for (a-c) different V_{AFe} waveforms.

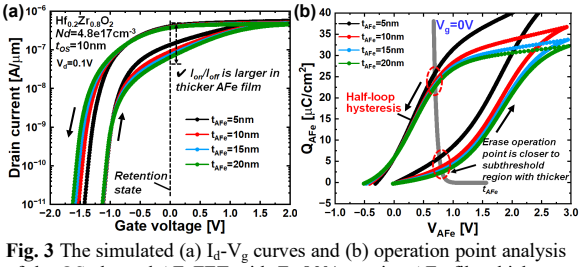

Fig. 3 The simulated (a) I_d-V_g curves and (b) operation point analysis of the OS channel AFeFET with Zr 80% varying AFe film thickness t_{AFe} at V_d = 0.1V

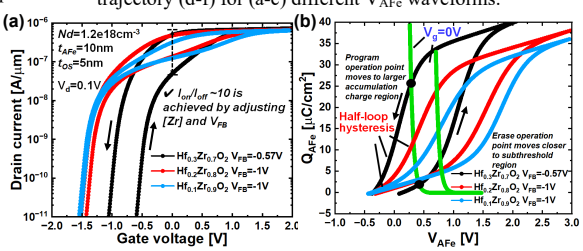

Fig. 4 The simulated (a) I_d-V_g curves and (b) operation point analysis of the OS channel AFeFET varying Zr concentration with V_{FB} adjustment at V_d = 0.1V.