Study on Variability of Carbon Nanotube Thin-film Transistor-based CMOS Differential Amplifiers

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[Introduction] Low-dimensional materials such as carbon nanotube (CNT) and MoS_2 are demonstrated to have great performance for thin-film transistors (TFTs) while including large characteristic variability[1]. Because of this, specialized circuit design that minimizes variation in circuit performance is necessary for analog circuit applications such as op-amps. Previous research[2] has reported an AC-coupled structure in PMOS-only circuits to suppress variation. However, PMOS-only circuits often have a more complicated structure and higher power consumption compared to CMOS-based circuits. In this research, we introduce a mismatch-suppressed (MS) structure in CMOS differential amplifier to reduce the effect of transistor variability. Variation suppression is demonstrated by circuit gain evaluation.

[Simulation] CMOS differential amplifier with MS structure is shown in Fig. 1(a). The MS structure in the broken line frame includes load transistors (M3, M4), resistor transistors (M5, M6), and AC short capacitors (C1, C2). For DC signal, gate and drain of load transistors are connected as diode-connected to show a low impedance. While for AC signal, load transistors are short-circuited by capacitors to become Zero-Vgs and show high impedance to give a high gain. The amplifier is constructed by CNT-TFT model and is simulated by HSPICE. Monte Carlo simulation based on Gaussian distribution function is applied to realize the transistor variability. The parameters are as shown in the table in Fig. 1(b).

[Result] Fig. 1(b) shows the comparison of gain distribution for MS structure and traditional current mirror (CM, a circuit without broken line frame in Fig. 1(a)). The MS structure can effectively increase mean gain by 3.7 times (from 15.3 to 26.7 dB) and decrease variation by 0.66 times (standard deviation from 7.4 to 3.8 dB) for N = 100 Monte Carlo simulation. While the 3-dB bandwidth keeps 36 kHz after applying MS structure. These results show that CMOS analog circuit design for large variability transistors becomes possible by using MS mentioned in this research.

[1] J. Hirotani *et al.*, *Nanoscale Adv.* **1**, 636 (2019)

[2] M. Sugiyama *et al.*, *Nat. Electron.* **2**, 351 (2019)

(a)

(b)

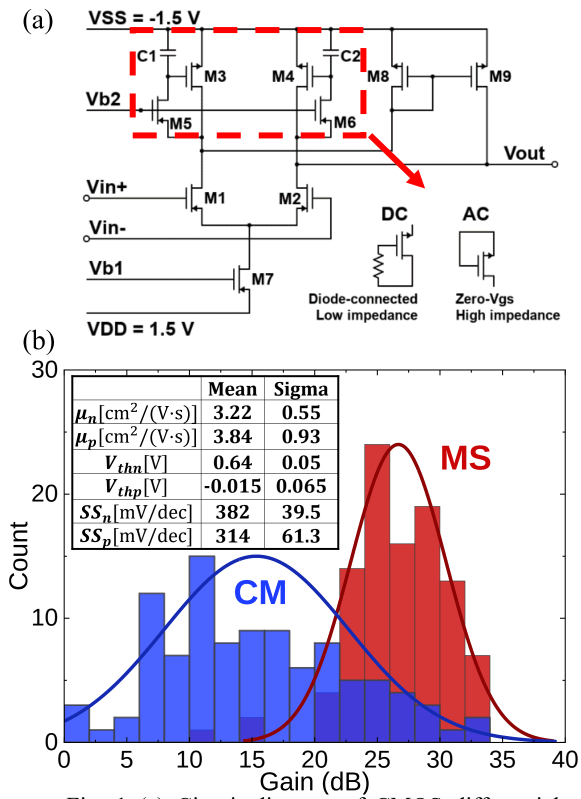

Fig. 1 (a) Circuit diagram of CMOS differential amplifier with MS structure. (b) Gain distribution comparison of MS and CM differential amplifier.