EOT scaling of top-gate MoS_2 FET below 1 nm

Univ. of Tokyo, ○Shuhong Li, Tomonori Nishimura, Kosuke Nagashio
E-mail: lishuhong@g.ecc.u-tokyo.ac.jp

Introduction

Progress in integrating high-κ oxides on top of 2D layered semiconductors is still tough due to the lack of suitable deposition method except ALD. Recently, we constructed a novel direct high-κ deposition system based on thermal evaporation in a differential-pressure-type chamber. The room temperature deposition of 5-nm Er_2O_3 with κ = ~18 on monolayer MoS_2 has been demonstrated with the successful reduction of equivalent oxide thickness (EOT) to 1.1-nm [1]. Although the further scaling of EOT is desirable, challenges to preserve the quality of insulator with reduction of insulator thickness thinner than 5-nm requires intensive exploration. Moreover, in order to further improve the subthreshold swing, the damage to the channel caused by deposition should be clarified.

In this work, dual-gate MoS_2 FET with 3.5-nm Er_2O_3 was fabricated to investigate the insulator quality, while the low temperature photoluminescence (LT-PL) and Raman measurements were addressed to investigate the defect formation after Er_2O_3 deposition.

Results & Discussion

MoS_2 channel with Ni/Au source and drain was defined by the CF_4/O_2 etching. Then, 3.5-nm Er_2O_3 was deposited as a full-cover insulator, followed by Au top gate metal formation. The photoresist was used as the passivation layer to avoid direct exposure to the atmosphere. I_{ds}-V_{tg} curve in **Fig. 1** clearly shows the on/off switching within 1 V. The κ value was then extracted as 12.9 by the V_{tg}-V_{bg} capacitive coupling, which is slightly degraded but remained relatively high compared with our previous work [1]. With the guarantee of high dielectric constant of Er_2O_3 film, the EOT is successfully reduced to 0.94-nm (**Fig. 2**). The results validate the potential for further EOT scaling by improving the κ value.

Raman and LT-PL measurements for 2-nm Er_2O_3 on monolayer MoS_2 were conducted to characterize the defect formation after the Er_2O_3 deposition. The defect-related bound exciton (X_B) located at 1.75 eV can be detected below 77 K when the defect density exceeds ~3×10^{12} cm^{-2} [3]. LT-PL spectrum of 2-nm Er_2O_3/MoS_2 at 4 K shown in **Fig. 3** indicates no obvious feature of X_B, supporting that the harmless deposition can be achieved by our deposition system. Furthermore, the Raman spectra in **Fig. 4** shows the recovery in terms of the intensity of two phonon modes (E^1_{2g} and A_{1g}) at different level after the removal of Er_2O_3 film by HCl etching. This suggests that the reduction of Raman intensity is not due to the defect formation but due to the suppression of phonon vibration, which is consistent with LT-PL result.

In conclusion, the dual-gate MoS_2 FET with EOT = 0.94 nm was achieved by harmless top gate deposition in this work. The optimization of insulator quality is strategic for the further scaling.

References

[1] H. Uchiyama, *et al.*, *small*, (in press).
[2] W. Li, *et al.*, *Nature Electron.*, **2**, 563 (2019).
[3] Y. Wan, *et al.*, *Nature Commun.*, **13**, 4149 (2022)

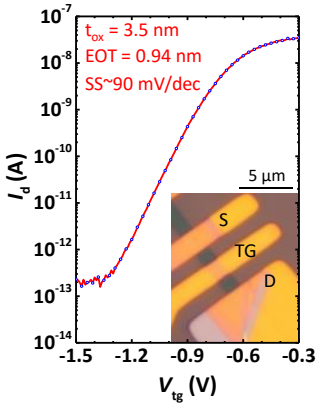

Fig. 1 *I-V* curve of dual gate Er_2O_3/MoS_2 FET.

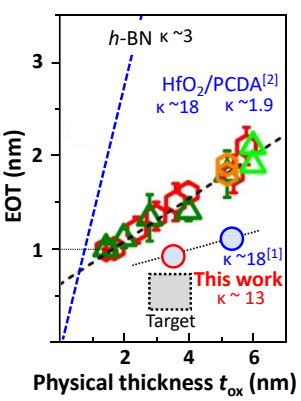

Fig. 2 EOT benchmark [1-2].

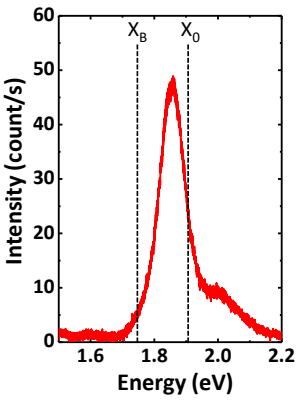

Fig. 3 LT-PL spectra of 2-nm Er_2O_3/MoS_2.

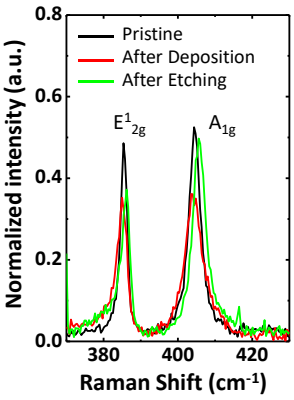

Fig. 4 Raman spectra before/after Er_2O_3 deposition and after HCl etching.