of GaAs Schottly Barrier Gate FM

S. MAI, Y, ISHIOKA, H. KUROHO, S. TAKAHASHI, and H. KOMERA Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo

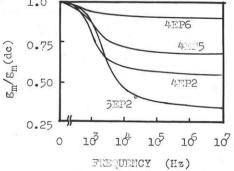
It has been shown that the GaAs Schottly barrier gate FET (SBFAT) is a device capable of microwave application and even outperforms Si npn transistors? So far, maximum frequency of oscillation as high as 50-40 GHz has been reported. The active region of a BETAT usually consists of a very thin (a few tenth of a micron) epitaxial film, which is liable to include unwanted defects and impurities. Therefore, it is important to have high quality epitaxial material in order to realize high frequency FAT's. In this paper we report several anomalous phenomena observed in GaAs FET's in the audio frequency range, which can be attributed to field-dependent trapping centers in the epitaxial films. The transconductance g_m is reduced at higher frequencies due to the trapping of conduction electrons, resulting in deterioration of microwave characteristics. Precautions to avoid incorporation of heavy metal impurities have resulted in FET's with satisfactory high frequency characteristics.

GaAs FMT's were fabricated using n-type epitaxial layers grown in GaAs/ ${
m AsCl_3/H_2}$ vapor transport system on semi-insulating substrate. Carrier concentration ranged from 2 to 4 x $10^{16} {
m cm}$, and thickness from 0.2 to 0.46 ${
m \mu m}$. Source and drain contacts were alloyed Au/Ge/Ni. The Schottky barrier gate was evaporated Mo-Au double layer, 2 ${
m \mu m}$ wide, being spaced 2 ${
m \mu m}$ apart from either source or drain. The aspect ratio ${
m Z/L}=250$.

Static characteristics of an FET showed hysteresis loops when displayed on an ordinary transistor curve tracer. Such a hysteresis has already been known in GaAs MOSFET and ascribed to deep-lying centers at insulator-semiconductor inter-

face. In contrast to the case of MOSTRT, gm decreased with increasing frequency and approached a high frequency limit at about 10 KHz, as shown in Fig. 1.

Drain saturation current $I_{\rm DSS}$, pinchoff voltage $V_{\rm p}$, and $g_{\rm m}$ were measured under
various biasing conditions. The results
obtained for a typical sample are summarized
in Table 1. Drain current and pinch-off
voltage are considerably larger for pulsed
biases than for dc.



* : an FET with 3 µm gate
Fig. 1 Frequency dependence of
normalized transconductance

The anomalous characteristics can not be explained by a simple deep donor (or acceptor) model for the trapping centers. Buch trapping centers would give rise to I_D and g_m larger and V_p lower at higher frequencies (or for pulsed bias). The nature of the trapping centers responsible to these anomalies is such that continuous (or dc) application of high field (due either to V_{DB} or V_{CB}) results in reduction in the number of conducting electrons. Therefore, the so-called field-enhanced trapping centers have to be called for to interprete the experimental results consistently. Furthermore, strongly field-dependent 1/f noise has been found, which provides another evidence for field-enhanced trapping centers.

The unilateral power gain given by

$$U = g_m^2 / \omega^2 c_{gs} g_d R_{eff}$$

is an important figure-of-merit, where \mathbf{g}_{d} is the channel conductance, $\mathbf{c}_{\mathbf{GS}}$ the gate input capacitance, and $\mathbf{R}_{\mathbf{eff}}$ the sum of all resistances in series with $\mathbf{c}_{\mathbf{GS}}$. Considerable deterioration in U results from reduction in $\mathbf{g}_{\mathbf{m}}$ due to the field-enhanced trapping. The high frequency characteristics are correlated with the low frequency anomalies as shown in Table 2.

For the purpose of improving quality of crystal and thereby the high frequency characteristics of FET's, we have employed EDTA treatment and vapor phase atching prior to growing epitaxial films. An FET fabricated on improved crystal, 4EP6, has been relatively free from the effects of deep level impurities and shown an fmax (frequency at which U = 1) of 19 GHz.

VDS	$d\mathbf{c}$	dc	pulse
V _{GS}	dc	pulse(hf)	pulse
g _m (m්ඊ)	26	18	22
I _{DSS} (mA)	80	-	120
V _p (V)	4.8	5.2	6.0

Table 1. \mathbb{G}_m , $\mathbb{I}_{\mathrm{ESS}}$, and \mathbb{V}_p under various biasing conditions

g _m (hf)	f _{max} (GHz)	
g _m (dc)	max.	typ.
0.58	11.0	6.5
0.69	11.0	9.0
0.90	15.0	12.0
	g _m (dc) 0.58 0.69	g _m (dc) max. 0.58 11.0 0.69 11.0

Table 2. Correlation between f_{max} and the degree of low frequency anomaly (as represented by $g_{n}(hf)/g_{n}(dc)$)

¹⁾ C. A. Licchti et al., Digest of Technical Papers, Int. Solid-State Circuits Conf., THPM 14.2, 158-159, Feb. 1972

²⁾ K. M. Drangeid et al., Electronics Letters, <u>6</u> 228-229 (1970)

³⁾ H. Becke et al., Solid State Electron., 8 819 (1965)

⁴⁾ B. K. Ridley and T. B. Matkins, J. Phys. Chem. Bolids, 22 155 (1961)