2-5 Self Aligned GaAs Schottky Barrier Gate FET using Preferential Etching

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The purpose of this paper is to apply a novel method of preferential etching to the self-alignment of Schottky Barrier FET. Etching rate of GaAs by solution of CH_3OH with few % Br. concentration is very small only at {111} A plane. Using this etching solution on (100) face of GaAs crystal through rectangular etching window, longitudinal edge parallel to $(0\bar{1}\bar{1})$ face, the etched profile has reverse mesa shaped structure.[1] This paper describes a self-aligned Schottky Barrier FET using the reverse mesa shaped structure.

To obtain high transconductance g_m and high source drain conductance at low voltage level g_o values it is essential to construct the FET with small channel length L and at the same time to reduce the series resistance R_s and R_d.[2] These severe requirements are satisfied by the method shown in Fig. 1 and Fig. 2, where the channel length L is determined by openning of the preferential etching window and the distance corresponding to the series resistance can be made small controlling the depth of preferential etching.

Fig. 2 shows the basic processes of fabrication. It starts from a N type GaAs epitaxial layer, having $10^{15} \sim 10^{16}$ carrier concentration and $3 \sim 4$ thickness, grown on the Cr-doped semi-insulating substrate by vapour phase epitaxial growth. Sulfur is diffused about 1 μ depth at surface from solid state Ga_2S_3 source[3] with additional atmosphere of Ga_2S_3 to suppress thermal conversion of N layer as shown in table 1. Overall impurity profile after diffusion is shown in Fig. 3. As shown in Fig. 2 (b), ohmic-metal of 9 : 1 wt.ratio Ag - Sn Alloy is evaporated about 1000 A thickness, followed by 500 c 15 min alloying in 10^{-5} Torr. vacuum. The Pt metal of 800 Å thickness is evaporated on Ag-Sn contact to protect from Br_2-CH_3OH etchant for the reverse mesa etching process. As shown in Fig. 2 (c), non preferential etching is carried out to isolate each region using H_2SO_4-H_2O_2-H_2O system. As shown in Fig. 2 (d), preferential etching by Br_2-CH_3OH system (5 wt. % Br_2) is carried out after defining the gate pattern on double layer of Al_2O_3 and photo-resist. As shown in Fig. 2 (e), Au metal of about 2000 Å thickness is evaporated for S.B. gate contact and bonding pads at the pressure of 1 x 10^{-7} Torr. using oil free system. The excess metal on the top surface is wiped off togeter with the photo-resist. By these process, SBD metal can be evaporated on a freshly etched surface and less damage on SBD after evaporation is expected. Final structure is shown in Fig. 4. $V_D - I_D$ characteristics of 5 μ channel length unit is shown in Fig. 5. The series resistance $R_s + R_d$ is estimated by the method in Fig. 6. These parameters are compared between the units without diffusion[2] and with diffusion and summarized in Table 2, which shows remarkable reduction of $R_s + R_d$ and increase of g_m. In Table 2, parameters of enhance type unit are also shown, which type is difficult to fabricate by other method. Typical unilateral

power gain of 5 μ unit at 1 GHZ calculated from S parameter is 7.4db.

It is shown the application of the preferential etch is effective way for the self-aligned GaAs FET. No critical alignment and no near by critical dimension of photo etching is necessary ; only small slit for etching mask is enough. For further improvement of the characteristics, the improvement of photo etch accuracy up to 1 μ ,[4] epitaxial growth for n^+ formation which improve the sharpness of the impurity profile, are effective.

We are grateful to Y.Harada, K.Mutoh and F.Matsumoto for experiments, F.Hayashi, Y.Hayashi and H.Tpshima for their advices.

(1) Y.Tarui et'al : Proc. 2nd Conf. on Sol. St. Devices (1970) 39p.
(2) Y.Tarui et'al : National Convention Record of I.E.C.E. of Japan, 1972, 1045p.
(3) S.Asai et'al : Proc. 3rd Conf. on Sol. St. Devices (1971) 231p.
(4) K.E.Drangeid et'al : Electronics Letter Vol.6,no.8,229p.

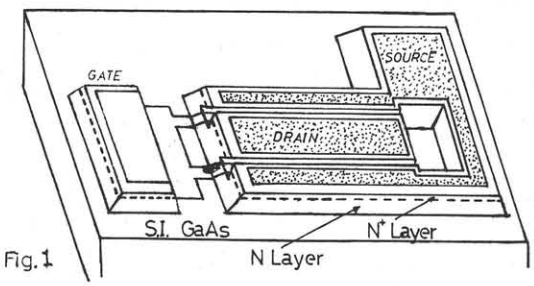

Fig.1

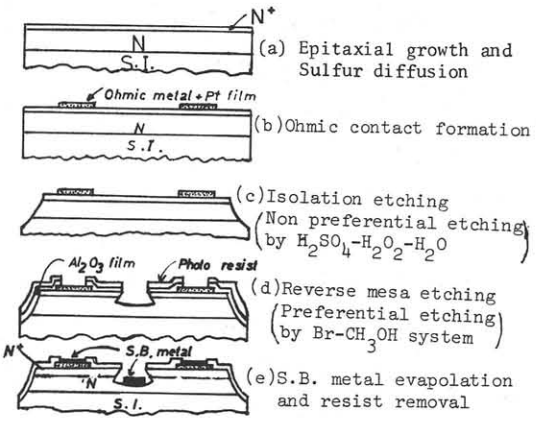

Fig.2 *Basic processes in fabrication of the* GaAs *S.B. FET*

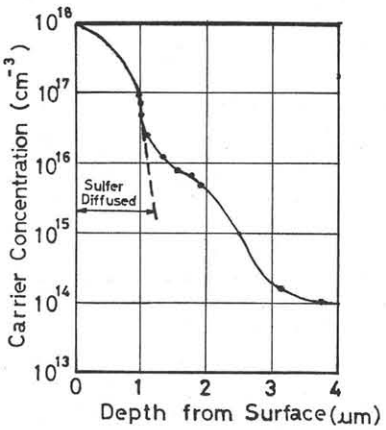

Fig. 3 Carrier Concentration Profile of Sulfur Diffused Epitaxial Layer.

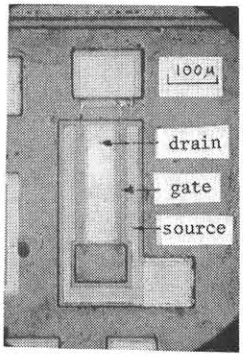

Fig.4

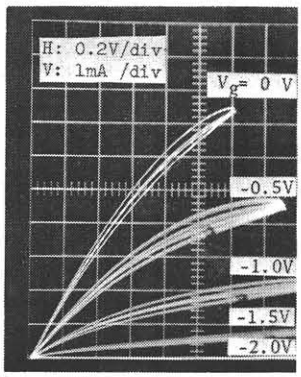

Fig. 5
(L=5μ. With N^+ Diffusion)

	Condition	Ambient	Diff. length	Results
1	850℃	Vacuum	1 μ	poor, N^+I
2	850℃	Ga_2S_3 gas	1 μ	good, N^+N

Table 1, Condition of Sulfur Solid(Ga_2S_3)Diffusion

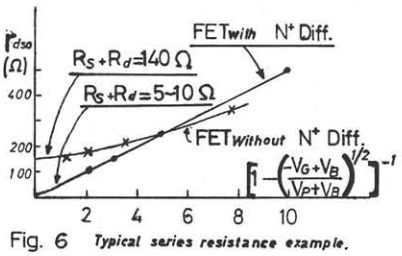

Fig. 6 *Typical series resistance example.*

	L(μ)	N_D(cm⁻³)	G_d(mℭ)	G_m(mℭ)	R_S+R_d	V_T
Depletion type (without N^+ Diff.)	5	$4X10^{15}$	3 (V_G=-5)	3 (V_G=-5)	230Ω	-18
Depletion type (with N^+Diff.)	5	$1X10^{16}$	10	8 (V_G=-0.5)	5~10Ω	-2
Enhancement type (with N^+Diff)	2	~$1X10^{15}$	0.8mℭ	1mℭ		0

Table 2 Typical Characteristics