5-3

Stacked-Gate Avalanche-Injection Type MOS (SAMOS) Memory

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In this paper we describe results of a study of injection, trapping and emission of electrons in a stacked-gate avalanche-injection type MOS FET (SAMOS) and a fully-decoded 256-bit ROM by the use of the new structure. This ROM is an extention of our previous AMOS[1] which has a single-gate narrow-channel transistor and of FAMOS[2]. A similar-type ROM was proposed by Tarui, Hayashi and Nagai[3].

The memory transistor has a double-gate structure (Fig. 1). The upper one is a control gate with an external contact, and the other is a floating gate isolated in the oxide. These gates are of polycrystalline silicon. The electron injection into the floating gate is accelerated and controlled by applying a positive bias on the control gate; the applied bias induces an accelerating field for electrons in the oxide and also reduces the depletion layer width at the surface near the drain junction which in turn reduces avalanche breakdown voltage. Hence, the SAMOS structure has a great advantage over the FAMOS concerning the "write" speed. In Fig. 2 are shown typical data on the threshold-voltage shift ΔV_{th} or the corresponding change ΔN_I in the induced carrier concentration in the inversion layer against the integrated time of a drain-voltage pulse. Generally, the "write" time of the SAMOS is over 1000 times shorter than that of the FAMOS. The SAMOS has another advantage that channel formation during the injection is prohibited by the presence of the control-gate field and no spurious channel current flows, and hence a smaller decoder transistor is possible, compared with the FAMOS. The retention of the stored charge in the floating gate is excellent; the half-life of the stored charge is estimated to be longer than 100 years at 125°C.

The erasing of the memorized transistor should mean discharge of the

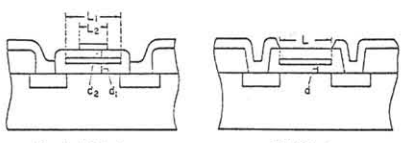

Fig. 1 SAMOS and FAMOS structures.

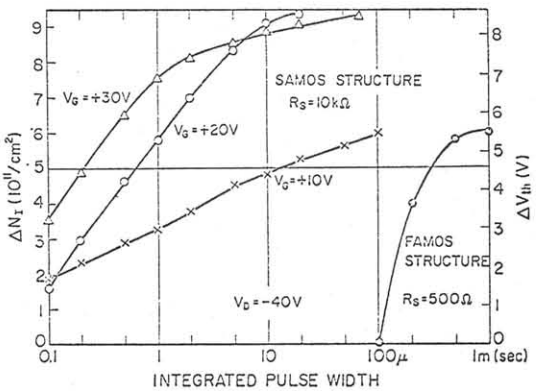

Fig. 2 "Write" characteristics of the SAMOS and FAMOS FET's. The structure parameters (see Fig. 1): $d_1 = 1600$ Å, $d_2 = d = 2000$ Å, $L_1 = 17\ \mu$, $L_2 = 7\ \mu$, $L = 7\ \mu$, $N_D = 1 \times 10^{15}$ cm^{-3}. Drain-voltage pulse = -40 V.

charge-stored floating gate. This can be done either optically (photoemission) or electrically (field emission). The erasing by photoemission is performed by irradiation of u. v. light of the energy above 4.2 eV, which means that photo-electrons are emitted from the valence band of the poly-Si to the conduction band of SiO_2. The shift in V_{th} more than 20 V was observed after an irradiation of 10^{18} photons of 5 eV. The "write" and "erase" cycle has no practical limitation.

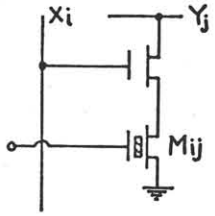

Fig. 3 A unit cell of a SAMOS memory matrix.

When a large positive voltage (e. g. 60 V for the sample shown in Fig. 2) is applied to the control gate, a tunneling current of Fowler-Nordheim type from the charged floating gate is observed, and the gate is neutralized. This can be used practically as an erasing operation, but possible "write" and "erase" cycles are limited to be less than 100, since the tunnel current becomes gradually smaller as the cycle is increased: An independent experiment leads to an interpretation that positive space charges are built in at the SiO_2-poly-Si interface and this would cause a thin potential barrier for the tunneling, and the tunneling electrons gradually compensate the positive charge, resulting in thicker barriers.

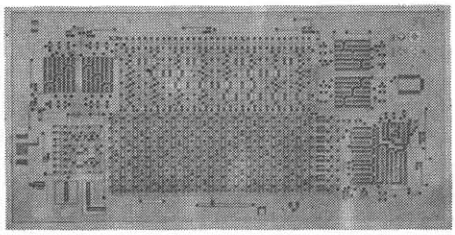

Fig. 4 A photograph of an LSI chip of a fully-decoded 256-bit SAMOS memory.

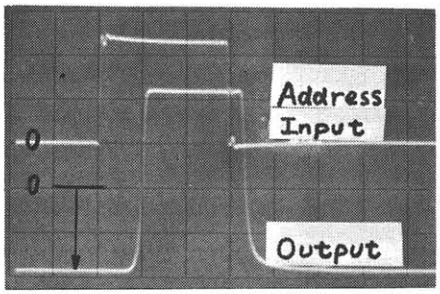

Fig. 5 Oscillograph traces of the address and output signals. Vertical: 2 V/div., Horizontal: 500 ns/div..

For an electrically programmable and rewritable ROM with above features, the unit cell consists of a SAMOS and a Si-gate MOS FET serving as the address selection transistor (Fig. 3). We have constructed a 256-bit SAMOS ROM utilizing the memory cell of this basic structure and conventional p-channel Si-gate MOS FET's for input, output and decoder circuits. A photograph of a test LSI chip is shown in Fig. 4. Oscillograph traces of the address and output signals are displayed in Fig. 5. The access time of this prototype ROM is about 500 ns. This can be readily decreased to 300 ns by a suitable design of the decoder transistors.

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2) D. F-Bentchkowsky: 1971 ISSCC Digest p. 80; Appl. Phys. Letters 18, p. 332 (1971).
3) Y. Tarui, Y. Hayashi and K. Nagai: Proc. 3rd CSSD, p. 155 (1971).