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A novel MOS-FET structure, with enhancement and depletion type gate region which we call E/D Gate, that realizes improved transconductance with $1\mu\text{m}$ channel and yet punch-through breakdown free MOS-FET has been proposed earlier by the authors.¹⁾²⁾ In this paper, the improved current-voltage characteristics of the device and the application to nano-second switching circuits will be discussed.

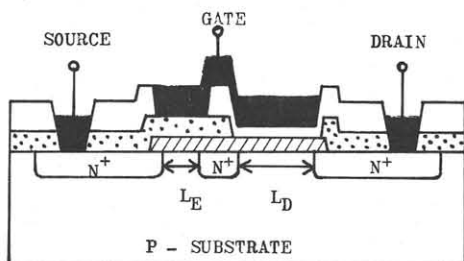
The proposed structure using alumina film technology is shown in Figure 1. The advantages of the structure are; (1) The drain current is mainly controlled by the enhancement region which has short channel length. (2) The punch-through breakdown voltage, on the other hand, is determined by the total channel length. (3) The breakdown voltage required for enhancement region is less than the absolute value of the threshold voltage of the depletion region.

The theoretical drain current as a function of punch-through breakdown voltage for conventional and E/D Gate MOS-FET are shown in Figure 2. It is obvious that the use of E/D Gate MOS-FET with $1\mu\text{m}$ enhancement region results in about 200 % improvement of the drain current. Figure 3 shows the fabricated devices. The experimental I_D - V_G characteristics of the device and conventional MOS-FET with the same channel length is shown in Figure 4. In the case of the gate voltage is 5 V, the I_D of the E/D Gate MOS-FET is $550\mu\text{A}$ whereas the I_D of the conventional one is only $220\mu\text{A}$. This result has a good agreement with the calculation in Figure 2. It should be noted that, in the case of low gate voltage, the transconductance of the E/D Gate MOS-FET is almost five times greater than that of conventional one.

The switching characteristics of the proposed device is also discussed. Figure 5 shows the comparison of the delay time between depletion load inverter circuits using E/D Gate MOS-FET for driver transistor and conventional ones. As shown in the figure, the circuit with new device shows the delay time of 8 ns/pF, whereas the conventional circuit has the delay time of 16 ns/pF, even if it has the depletion type load.

References

- (1) M. Nagata et al. ; IEDM late news (1971)
- (2) M. Nagata et al. ; A Short Channel MOS-FET of New Type ; SSD71-39 (1971)



L_E = CHANNEL LENGTH OF E-MODE REGION

L_D = CHANNEL LENGTH OF D-MODE REGION

SiO_2 (500Å) Al_2O_3 (2000Å) PSG (700Å)

FIG.1 CROSS SECTIONAL STRUCTURE OF E/D GATE MOS-FET.

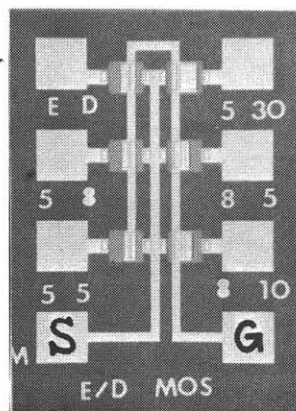


FIG.3 EXPERIMENTAL DEVICES.

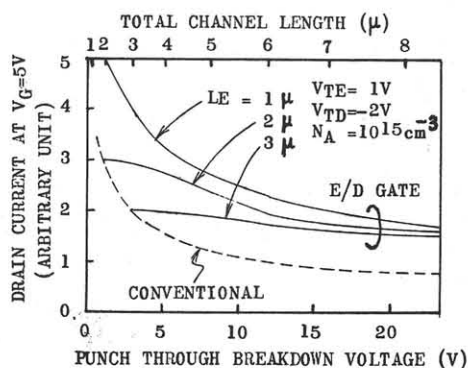


FIG.2 COMPARISON OF DRAIN CURRENT BETWEEN CONVENTIONAL AND E/D GATE MOS-FET AS A FUNCTION OF BREAKDOWN VOLTAGE.

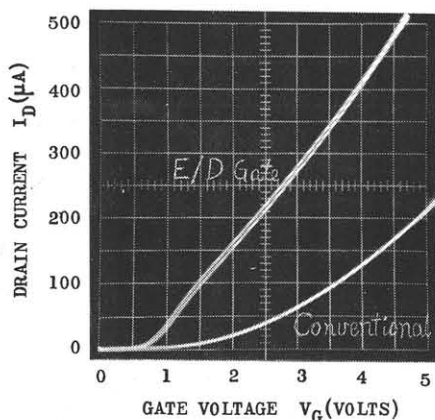


FIG.4 EXPERIMENTAL I_D - V_G CHARACTERISTICS OF E/D GATE AND CONVENTIONAL MOS-FET WITH THE CHANNEL LENGTH OF 31 μm .

$L_E = 3 \mu\text{m}$, $V_{TE} = 0.8 \text{ V}$

$L_D = 28 \mu\text{m}$, $V_{TD} = -2.4 \text{ V}$

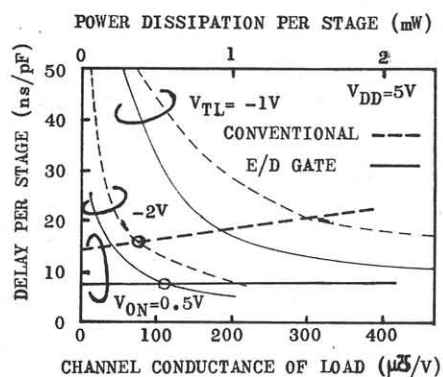


FIG.5 DELAY TIME VERSUS β OF LOAD FOR DEPLETION LOAD INVERTER CIRCUITS USING CONVENTIONAL AND NEW DEVICE WITH SAME DIMENSIONS FOR DRIVER. (V_T OF DRIVER IS 1 VOLT)