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A 1024 bit N-Channel MOS high speed RAM

J.Nogi, K.Miyasaka, S.Enomoto

FUJITSU LIMITED

1015 Kamikodanaka Kawasaki JAPAN

In recent years, MOS Large Scale dynamic Read/Write memories became available to applied to Main Frame Memory Systems. Technology of MOS dynamic Read/Write memory used in the above field has been steadily improved in regard to the access time and bit density.

A 1024 bit MOS dynamic Read/Write memory (MB8201) with access times of less than 80nS has been designed and completed. Table 1 shows principal characteristics of the MB8201.

1024bits;1024 words by 1 bit
Access time 80nS.
Cycle time 160nS.
Clock level "1" +10.4V-+11.6V
Active power 0.15mW/bit
Power supplies +12V,+5V,-5.2V
Refresh interval 500uS.

Table 1

Logical "1" levels of address and clock terminals are only 10.4V(min.) with respect to V_{SS} terminal, while those of many other cases of MOS dynamic RAM are 16 - 20V. Fig 1,2 show operation immunity to clock levels and power supply voltages. High speed ($t_{access} \leq 80nS$) has been achieved with several considerations. One of them is to use N-Channel Al Gate MOS technology with fine pattern photo-process instead of Si-Gate MOS technology. Although Si-Gate technology is suitable for increasing integration density, it is not for high speed devices, because the resistance of Poly-Si layer gives a considerable effect in comparison with that of Al or other metals. The other one is to use Modified Bootstrap circuits for decoding and driving circuits as follows. In Fig 3(a), when $\emptyset_A$ is active, C_2 is charged up to high level and Q_2 turns "ON". As $\emptyset_A$ goes low, however, the charge stored on C_2 can not leak out and Q_2 is kept "ON". By making $\emptyset_B$ high, C_1 C_2 are charged gradually through Q_2 so that V_{out} rises and the gate potential of Q_2 is raised simultaneously.

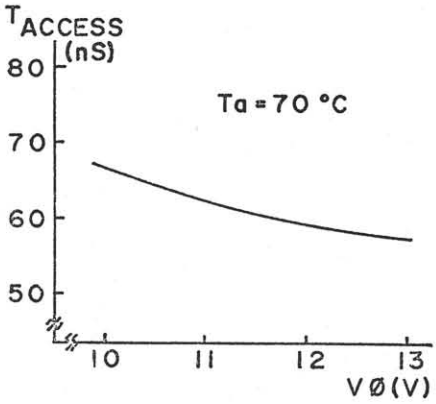


Fig 1 t_{access} vs $V_{\emptyset}$

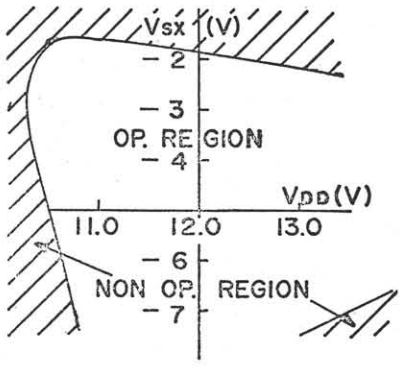
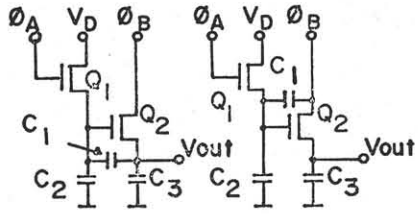


Fig 2 Operation immunity

With this operation scheme, interrelation C_1, C_2 and C_3 were set to obtain sufficient gate level of Q_2, V_{out} would be nearly equal to $V_{\phi B}$. Without large $B(=W\cdot e_{ox}\cdot u/L\cdot t_{ox})$ of Q_2, the transient response of V_{out} for ϕ_B will not be so fast in this case.

Modified Bootstrap circuit (with additional C_1 between gate and drain of the Q_2, used in MB8201), shown in Fig 3(b), will be able not only to raise up the gate potential of Q_2 but also to gets faster transient response of V_{out} for ϕ_B. Because, gate potential of the Q_2 is raised directly by $V_{\phi B}$ and conductance (gm) of the Q_2 turns to maximum value quickly.



(a) usual (b) modified

Fig 3 Bootstrap circuit

V_{out} transient response of both usual and modified Bootstrap circuits are calculated approximately as follows.

For usual Bootstrap circuit

$$V_{out}(t)=\frac{V_{eff}}{A(1-C_R)}-\frac{2C_0V_{eff}}{B_{eff}t\,V_{eff}(1-C_R)^2+2A(1-C_R)C_0}$$

For modified Bootstrap circuit

$$V_{out}(t)=V_{eff}+C_RV_D-\frac{2C_3(V_{eff}+C_RV_D)}{B_{eff}t(V_{eff}+C_RV_D)+2C_3}$$

where

$V_{eff}=V_D-V_{PQ1eff}-V_{PQ2eff}$

A; constant value

$C_0=C_1(C_R-1)+C_3$

$C_R=C_1/(C_1+C_2)$

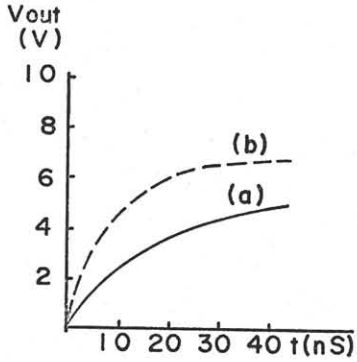


Fig 4 calculated waveform

The results of numerical calculation of these expression are shown in Fig 4 and observed wave forms under same condition are shown in Fig 5.

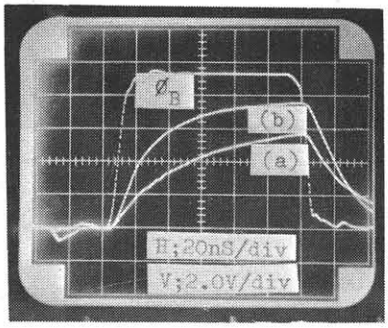


Fig 5 observed waveform

This device can be packaged in a ceramic hermetically sealed type of either DIP-24 pin or QIT-24 pin packages as shown in Fig 6.

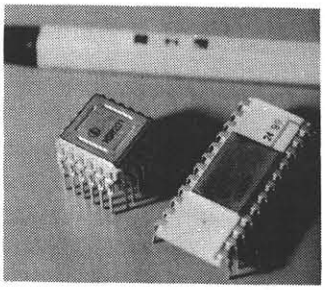


Fig 6 The MB8201