A 1024 bit N-Channel MOS high speed RAM

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In recent years, MOS Large Scale Dynamic Read/Write memories became available to applied to Main Frame Memory Systems. Technology of MOS dynamic Read/Write memory used in the above field has been steadily improved in regard to the access time and bit density.

A 1024 bit MOS dynamic Read/Write memory (MR8201) with access times of less than 80ns has been designed and completed. Table 1 shows principal characteristics of the MR8201.

Logical "1" levels of address and clock terminals are only 10.4V (min.) with respect to $V_{GS}$ terminal, while those of many other cases of MOS dynamic RAM are 16 - 20V. Fig 1, 2 show operation immunity to clock levels and power supply voltages. High speed ($t_{\text{access}} \leq 80\text{ns}$) has been achieved with several considerations.

One of them is to use N-Channel Al Gate MOS technology with fine pattern photo-process instead of Si-Gate MOS technology. Although Si-Gate technology is suitable for increasing integration density, it is not for high speed devices, because the resistance of Poly-Si layer gives a considerable effect in comparison with that of Al or other metals. The other one is to use Modified Bootstrap circuits for decoding and driving circuits as follows.

In Fig 3(a), when $\phi_A$ is active, $C_2$ is charged up to high level and $\phi_2$ turns "CH". As $\phi_A$ goes low, however, the charge stored on $C_2$ can not leak out and $\phi_2$ is kept "CH". By making $\phi_B$ high, $C_1$ and $C_2$ are charged gradually through $C_2$ so that $V_{out}$ rises and the gate potential of $\phi_2$ is raised simultaneously.

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Table 1

<table>
<thead>
<tr>
<th>1024bit</th>
<th>1024 words by 1 bit</th>
<th>Access time 80ns.</th>
<th>Cycle time 160ns.</th>
</tr>
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<tbody>
<tr>
<td>Clock level &quot;A&quot;</td>
<td>$+10.4V - +11.6V$</td>
<td>Active power 0.15mW/bit</td>
<td>Power supplies $-12V$, $+5V$, $-5V$.</td>
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<tr>
<td>Refresh interval</td>
<td>500us</td>
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<td></td>
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</tbody>
</table>

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Fig 1 $t_{\text{access}}$ vs $V_\phi$

Fig 2 Operation immunity
With this operation scheme, interrelation $C_1$ and $C_2$ were set to obtain sufficient gate level of $Q_2$, $V_{out}$ would be nearly equal to $V_{Z_B}$. Without large $R = \frac{W}{L} \cdot I_{ox}$ of $Q_2$, the transient response of $V_{out}$ for $V_{B}$ will not be so fast in this case.

Modified Bootstrap circuit (with additional $C_1$ between gate and drain of the $Q_2$, used in MB8201), shown in Fig 3(b), will be able not only to raise up the gate potential of $Q_2$ but also to get faster transient response of $V_{out}$ for $V_{B}$. Because, gate potential of the $Q_2$ is raised directly by $V_{PB}$ and conductance ($gm$) of the $Q_2$ turns to maximum value quickly.

$V_{out}$ transient response of both usual and modified Bootstrap circuits are calculated approximately as follows.

For usual Bootstrap circuit

$$V_{out}(t) = \frac{V_{eff} - \frac{2C_2V_{eff}}{A(1-C_2)}}{A(1-C_2)^2 + 2A(1-C_2)C_0}$$

For modified Bootstrap circuit

$$V_{out}(t) = V_{eff} - \frac{C_1V_D - \frac{2C_2(V_{eff} + C_2V_D)}{V_{eff}(V_{eff} + C_2V_D) + 2C_2}}{V_{eff}(V_{eff} + C_2V_D) + 2C_2}$$

where

$$V_{eff} = V_D - V_{PP}$$

$A$: constant value

$C_0 = C_1 - C_2$

$C_R = C_1/C_2$

The results of numerical calculation of these expression are shown in Fig 4 and observed waveforms under same condition are shown in Fig 5.

This device can be packaged in a ceramic hermetically sealed type of either DIP-24 pin or QIT-24 pin packages as shown in Fig 6.