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P^+-Graded Junction-N^+ High-Efficiency Avalanche (TRAPATT) Diode*

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Computer simulations have been carried out for the operation of punch-through P^+-graded junction-N^+ (P^+-G-N^+, Fig. 1a) type silicon Trapatt diodes. Previous theoretical studies have concentrated on abrupt junction diodes, yet most successful Trapatt diodes utilize graded junctions. The P^+-G-N^+ type diode can take high bias-current without burn-out[1] and also produces higher peak RF power than abrupt P^+-N-N^+ type diodes (e.g., Table 1). The graded diodes exhibit a $V^{-1/3}$ capacitance dependence at low reverse-voltages and have a relatively constant value of capacitance at high voltages. These diodes are fabricated by a deep diffusion process[1] and a two-point probe profile measurement has confirmed the punch-through P^+-G-N^+ structure.

In the simulation, a reverse-biased diode in series with a bias source terminates a transmission line having a characteristic impedance Z_o. A positive pulse wave (represented by a half-sine wave) is incident through the transmission line on the diode[2], and the diode reflects an amplified negative pulse wave. Given the incident pulse, the program solves for the reflected voltage, diode voltage, current, power, and efficiency. The system of equations used to describe the diode express the devices physics (impact ionization, etc.) at mesh points within the graded region, and the program calculates the interaction between the diode and transmission line circuitry.

Fig. 1 shows the transient behavior leading to the formation of trapped plasma. Initially the electrical field peaks at the center of the graded region, thus the electron hole plasma generation begins at the middle of the graded region (Fig. 1a). As the plasma grows, it shifts toward the N^+ side, approximately 60% of the way across as shown in Fig. 1c. This shift occurs because electrons drift toward the N^+ region, and their ionization rate is greater than the ionization rate of holes. The optimum frequency of operation for P^+-N-N^+ diode (Fig. 2) is given by $f(GHz) \sim 7/W_n(\mu m)$.

In order to understand the diode operation more clearly, consider the P^+-G-N^+ diode as two series-connected diodes (similar to double-drift Impatt diodes) with different depletion-layer widths. The optimum frequency will be determined by the diode having the widest active region; $f \sim 7/0.6\ W_G \sim 12/W_G$ (Fig. 2). Therefore, the optimum W_G for graded diode is greater than the optimum W_n for abrupt diode at a given frequency. Since the diode breakdown voltage V_B increases with W and the output power density is approximately proportional to V_B^2, the RF output power density for graded diode is greater than that for abrupt diode. For a given output power density, the bias current density for graded diodes is smaller than that for abrupt diodes. Figure 3 and Table 1 show a comparison between calculated diode performance and experimental results obtained on several diodes. Note that the agreement is excellent.

The simulation has revealed that the product AZ_o, diode area times transmission line surge impedance, has an optimum value for best operating efficiency. This is because the time constant

in charging diode capacitance ($\sim Z_o A/W$) must be in the order of the rise time of the pulse waves. Fig. 2 indicates that, for a given frequency f and line impedance Z_o, the optimum diode area A for graded diodes is 25-65% higher than that for abrupt diodes. Thus, graded diodes have power capability advantage over abrupt diodes (note that the choice of low line impedance for JP118 in the table allowed further increase in the diode area and therefore resulted in an increase in output power).

In conclusion, the high output power density and large diode area, resulting from the choice of wide depletion-layer width, gives rise to the high peak power capability of graded junction diodes. The experimental results presented are in excellent agreement with the theory.

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	ABRUPT JUNCTION		GRADED JUNCTION	
	EXPERIMENT[3] HF-7, D=.13mm	SIMULATION	EXPERIMENT[4] JP118, D=.64mm	SIMULATION
Frequency f (GHz)	3.35	3.3	3.3	3.3
Factor n in $C \sim V^{-n}$	0.50	0.50	0.356	0.333
Depletion Layer Width W(μm)	1.76	2.0	4	4
Impurity Gradient a (atoms/cm^{-4})	—	—	4×10^{19}	4×10^{19}
Impurity Density Nd (atoms/cm^{-3})	1.3×10^{15}	1.5×10^{15}	—	—
Diode Area A (cm^2)	1.25×10^{-4}	1.25×10^{-4}	3.12×10^{-3}	3.12×10^{-3}
Characteristic Impedance Z_o (Ω)	50	60	4	4
Area-Impedance Product AZ_o (Ω-cm^2)	6.25×10^{-3}	7.5×10^{-3}	1.25×10^{-2}	1.25×10^{-2}
Bias Voltage V_{bias} (V)	40	40	90	90
Current Density J_D (KA/cm^2)	8.0	8.1	2.9	2.8
Efficiency η (%)	26	28	25	26
Output Power P_R (W)	10.3	10.5	200	205

Table 1 Comparison of the performance at 3.3 GHz between experiments and simulations.

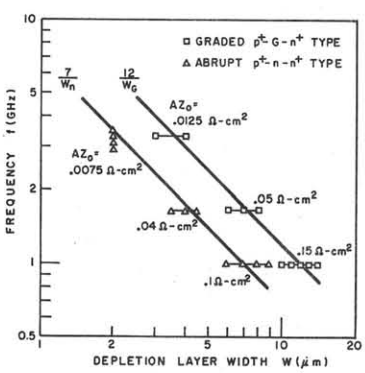

Fig. 2 Optimum frequency of operation as a function of depletion-layer width. The AZ_o product used in simulation is listed for each operating point

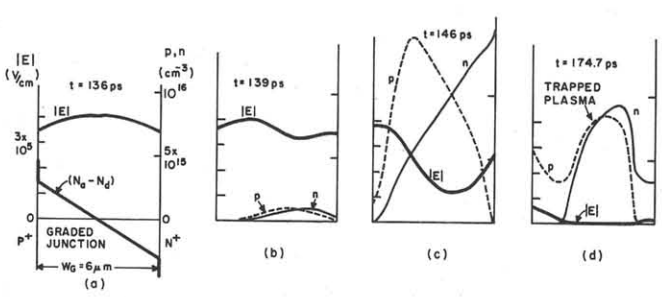

Fig. 1 Impurity profile of P^+-Graded Junction-N^+ diode and formation of trapped plasma. f = 1.65 GHz, a = 10^{19}cm^{-4}, V_{bias} = 110V.

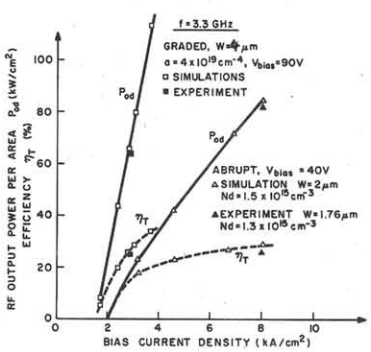

Fig. 3 Output power density and efficiency as a function of diode current density.