10-6 Negative Differential Resistance and Thermal Effect in Silicon MOS Field-Effect Transistors

Hiroyuki SAKAKI* and Takuo SUGANO

Department of Electronic Engineering,
University of Tokyo, Hongo, Tokyo, 113, Japan

I. Introduction

It was found by Katayama et al that Si MOS transistors exhibit a negative differential resistance (NDR) when measured by a pulse method at 4.2K.[1] Later Murayama et al proposed a semi-empirical model and attributed the NDR to a scattering mechanism whose scattering rate increases with electron energy.[2]

In the present work, this NDR effect is re-examined by measuring the current-voltage characteristics on MOS transistors of various channel lengths L and widths W with a refined pulse method. From the measured data, we shall show that the NDR is ascribable to a thermal effect (temperature rise in the channel due to Joule heating) rather than to an ad hoc scatterer of Murayama et al.

II. Experimental Method and Results

A square voltage pulse v(t) with the pulse width of 100 ns is applied to the drain electrode of an FET, which is immersed in liquid helium, and the current response i(t) is measured by a sampling oscilloscope. By sampling i(t) and v(t) at some time t_s from the front edge of a square pulse, drain-current $i(t_s)$ versus drain-voltage $v(t_s)$ characteristics are obtained. Typical results are shown in Figs. 1 and 2 for the channel length of 10μm and 100μm, respectively.

(A) NDR of short-channel devices It is shown in Fig. 1 that the NDR of a short-channel FET is small and appears when V_d exceeds 10V and when V_g is lower than 40V (this corresponds to electron concentration N_s of $10^{12}/cm^2$). These features are found common to all the crystal surface orientations studied, namely (111), (110), and(100), and to the current-flow directions. When samples of longer channel are tested, the NDR becomes more marked. This geometrical dependence and the insensitivity to crystallographic orientation suggest that the NDR is associated with the thermal effect which depends on dimensions.

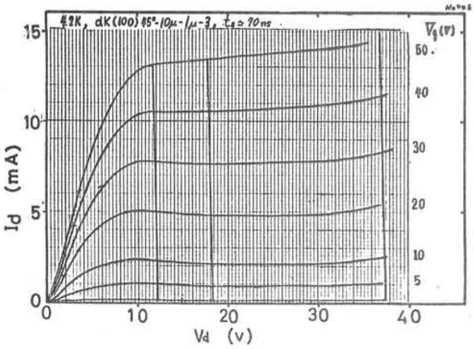

Fig. 1 Drain current I_d versus drain voltage V_d measured at 4.2K on a short-channel FET with L=10μm W=100μm, and d_{ox}=1μm, fabricated on a (100) surface of p-type silicon. Sampling time t_s is 70 ns.

* Present Address, Institute of Industrial Science, University of Tokyo, Roppongi, Tokyo, 106, Japan

(B) NDR of long-channel devices A long-channel FET ($L=100\mu m$) exhibits a large NDR as shown in Fig. 2. Note that the electric field required for the onset of NDR is about $2\times10^3 V/cm$ for $L=100\mu m$ and is much lower than that for $L=10 \mu m$. For t_s smaller than 70 ns, higher drain voltage is required to set on the NDR. In Fig.3, the time dependence of I_d at V_g = 70V is shown for various value of V_d. It is noteworthy that i(t) is composed of a high-current state and a low-current state. If the sampling point, which is indicated by a circle on each curve in Fig. 3, is in a high-current state, as in the case of curve (7), then the I_d-V_d characteristics in Fig. 2 exhibit a positive resistance. When the drain voltage is chosen higher than that of curve (7), then the sampling point falls on the transition region from the high- to the low-current state as in the case of curves (5) and (6). In such case, the NDR is observable in Fig. 2.

III. Discussions

By solving an equation of thermal conduction, it can be shown that the rise of temperature in the channel is typically of the order of 10^oK. In case the heat path in the real MOSFET is not as ideal as we assumed, it is probable to have a rise of several tens of degrees. In such case, the rise of T may lead to the decrease of electron velocities and consequently lowers the drain current.

For a device with $L=10\mu m$, I_d is limited by the saturation velocity v_s of electrons for $V_d > 10V$. In such case the rise in T can be shown to lead to an NDR because $v_s^{-1}(\partial v_s/\partial T)$ is approximately $-10^{-3}/^oK$, as shown by Fang and Fowler[3].

For a long-channel FET, in which velocity saturation effect is negligible, the current is affected by the temperature rise through the temperature dependence of mobility. Most of the data described in II(B) can be explained by assuming μ to be constant for low temperatures and to decrease with T for high temperatures.

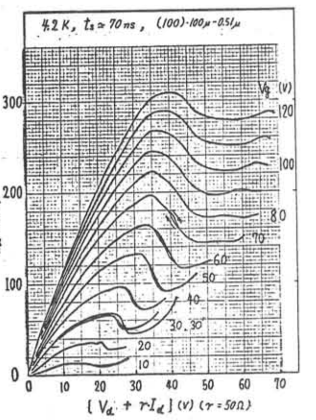

Fig. 2 I_d versus V_d+rI_d measured at 4.2K on an FET with $L=100\mu m$, $W=1500\mu m$, and $d_{ox}=0.51\mu m$. (100)surface, t_s=70 ns, r=50Ω

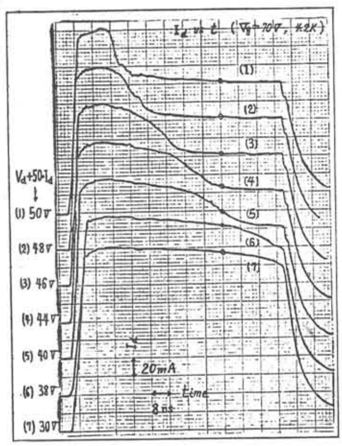

Fig. 3 I_d versus time t measured at 4.2K on a sample of Fig. 2 for V_g= 70V. Pulse width is 100ns. A circle on each curve indicates the point of sampling used for Fig. 2.

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2) Y.Murayama, Y.Kamigaki and E.Yamada, J.Japan Soc. Appl.Phys. 41S('72)133.
3) F.F.Fang and A.B.Fowler, J.A.P. 44 ('70) 1825.