11-5 INVITED: Electrically Reprogramable Nonvolatile Semiconductor Memory

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Electrically reprogramable nonvolatile semiconductor memories have received considerable attention in recent years for the demands of an analogue memory, computer microprogramming application and a substitute for the capability of magnetic memories.

MNS and MNOS[1] as in Fig.1 have been the subject of extensive investigation for several years, and now the physics of failure of reprograming over 10^6 times is under discussion. MAS[3] and MAOS[4] memory are also can be electrically reprogrammable.

Another approach is the use of a floating gate in the insulator. Floating gate has well defined physical structure and possibly has better designability compared with the traps in insulators. Floating gate for a nonvolatile memory element was first proposed by Khang and Sze.[5] In their proposed structure, floating gate is deposited over a very thin (50 A) layer of dielectric, to allow charge transport by tunneling from the substrate. To avoid the leakage from a floating gate to substrate through thin insulator film, floating gate of small metal particles[6] or polycrystal silicon partly oxidized[7] on thin film of SiO_2 are proposed.

On the other hand, avalanche injection of electrons into insulating SiO_2 using MOS structure was observed up to current density as high as 10 mA/cm^2 [8][9][10] Using this injection current, memory with floating gate embeded on thicker(1000 A) oxide was realized by a FAMOS device[11] as shown in Fig.2. The device, however, is not yet electrically rewritable. The electrically reprogrammable FAMOS structure was realized by providing two injection mechanism; namely for electrons and holes.[12] One method is two junction type where the p^+n and n^+p junction are constructed under the double gate structure. One other way of electrical erasing in a stacked-gate structure is done by control of gate bias V_G changing the balance of electron transfer from substrate to floating gate and floating gate to control gate. Avalanche injection is also applied to MNOS structure.[14]

An improved memory device of two injection mechanism is shown in Fig.3(a). In this structure holes are injected by the fringing field drain junction breakdown. For the electron injection, gate and drain are biased positive, then the surface of the p region under gate is bend as shown in Fig.3(b). When V_{G2} and V_D are both high enough for the breakdown at the depleted region, high energy part of the electrons in breakdown current are injected to the floating gate. In this new mode of operation, fairy uniform plane injection is expected; we call this mode as a plane injection mode.

Minimum gate voltage necessary for avalanche breakdown BV_{GB} for the plane injection, e.g. electron injection in the case of Fig.3(a), can be estimated by next equation.

$$BV_{GB} = BV_{CB} + 2\phi_{FB} + \frac{T_{OX}}{\varepsilon_{OX}} \sqrt{2q\varepsilon_{Si} N (BV_{CB} + 2\phi_{FB})}$$

where BV_{CB} is breakdown voltage of the p region in Fig.3(a) as a one sided step junction, T_{OX} is total thickness of gate oxide. Fig.4 shows the results of calculation and data measured on MOS diode of oxide thickness 1000 A.

In the case of fringing field injection by pn junction, e.g. hole injection in Fig.3(b), there exist various path between n^+ region and the gate, through various length of depleted p region. Then the avalanche breakdown voltage between n^+ region and the gate was calculated using variable path length of p region. The results of calculation in Fig.5 shows minimum voltage exist around 0.1 ~ 0.3 μ depending on oxide thickness.

It is noted that the minimum voltage with same SiO_2 thickness in Fig.4 and 5 are nearly same

showing the limits of avalanche method. A method to break the limitation is use of minority carrier injection by forward biased pn junction as shown in Fig.6.

The memory cell of Fig.3(a) was fabricated. The basic operation of the memory can be understood by the relation between the current through the oxide and potential of the floating gate. Fig.7 shows the results of the measurement done with a additional lead attached to the floating gate which is otherwise floating. Fig.8 shows the electron injection efficiency, the ratio of gate current to drain current, as a function of gate bias.

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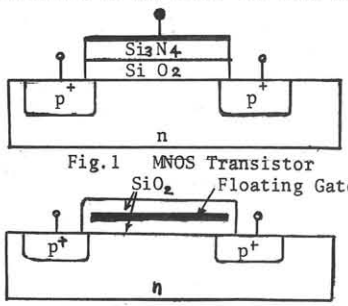

Fig.1 MNOS Transistor

Fig.2 FAMOS Transistor

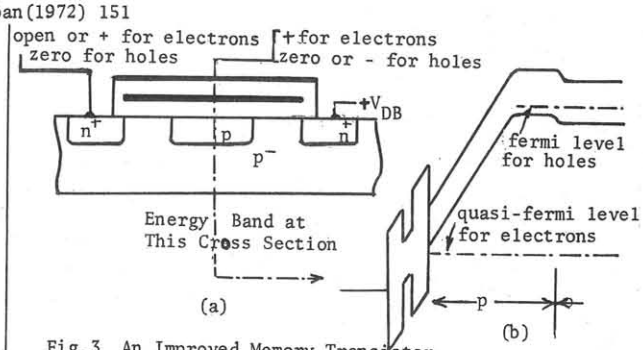

Fig.3 An Improved Memory Transistor

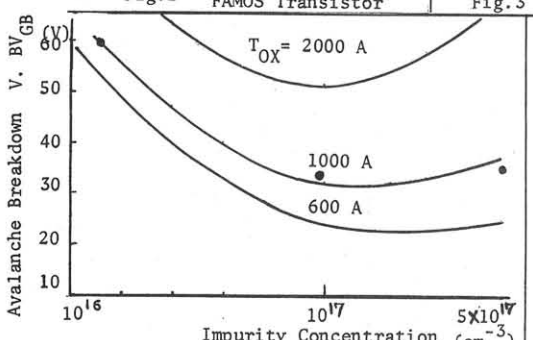

Fig. For Plane Injection

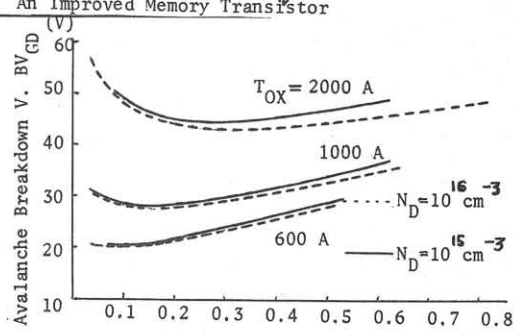

Fig.5 For Fringing Field Injection

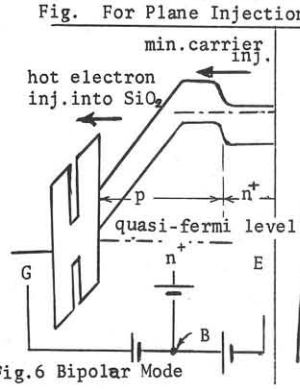

Fig.6 Bipolar Mode

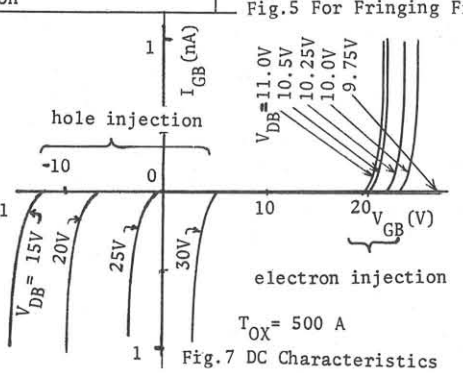

Fig.7 DC Characteristics

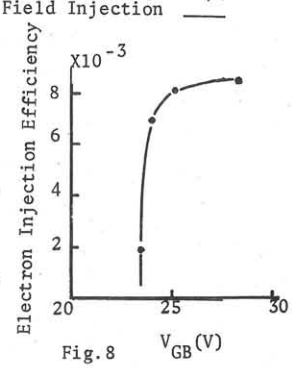

Fig.8