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ELECTRICALLY ERASABLE NON-VOLATILE OPTICAL MEMORY FOR VISIBLE AND INFRARAD LIGHT PATTERN

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INTRODUCTION

One of hopeful ways to realize direct memorization of optical image is injection of photo-generated carriers through insulator into a potential well within the insulator, such as a floating gate or interface traps between two kind of insulators.

Injection into a insulator from semiconductor surface of high energy carriers generated by high energy photon (e.g. ultraviolet) is realized by simple structures[1] and has been used as a method to determine barrier energy between insulator and semiconductor[2]. To inject carriers generated by visible light through a thick insulator over a barrier, following two principles must be considered:

1. Carriers are generated in higher potential part of semiconductor surface than barrier potential.
2. The higher potential part of semiconductor is made as near as possible to insulator-semiconductor interface to prevent energy decay of carriers.

Because of high energy carriers will decay to $\exp(-d/L_0)$ of initial number, where d represents distance between the higher potential part of semiconductor and insulator-semiconductor interface as shown in Fig.1. L_0 denotes attenuation length of carriers and reported as $L_0 \simeq 45$ Å for electrons in Si by Berglund et al.[3]

PROPOSAL of a DEVICE STRUCTURE and EXPERIMENTAL RESULTS

One of device structures realizing the above principles is a transparent poly-silicon floating gate FET as shown in Fig.2. There are two possible operating modes to use this device as a optical memory. One is injection of photo-excited carriers into the floating gate using drain to gate fringing field lower than avalanche critical field but high enuogh to give the carriers high potential and reduce the distance "d". The other is the use of reverse biased surface depletion layer under the floating gate biased to delete or invert the substrate surface.

An experimental n-channel device shown in Fig.3 was fabricated by using silicon gate technology to confirm the above proposal. Fig.4 shows charging time constant, τ of the floating gate with constant gate2 to drain bias under illumination of a tungsten lamp through a color filter VR63. The charging time constant, τ was measured as a time for the threshold voltage shift measured from the gate2 to reach 63% of the final value. The threshold voltage shift, ΔV_{th} was non-volatilely memorized and for measurement of the respective time constant, charge stored in the floating gate was electrically erased by injection of holes generated by avalanche breakdown of drain junction. d in Fig.1 is given by

$$d = \sqrt{\frac{2\varepsilon_{se}}{qN}}\left\{\sqrt{V_{DB} + 2\phi_{FB}} - \sqrt{V_{DB} + 2\phi_{FB} - E_B^*/q}\right\} \qquad \text{--- (1)}$$

$$E_B^* = E_B - h\nu + E_G \qquad \text{--- (2)}$$

and charging current to the floating gate, I_{G1} is propotional to $\gamma_d = \exp(-d/L_0)$ of photo-excited current I_{ph} in the semiconductor surface, The exponential dependence on the drain to substrate bias, V_{DB} of charging time constant is reasonably explained as,

$$\tau = \frac{C_{G1}\Delta V_{th1}}{I_{G1}} \propto \frac{C_{G1}\Delta V_{th1}}{I_{ph}} \exp(d/L_0) \qquad \text{--- (3)}$$

where, C_{G1} and ΔV_{th1} denote capacitance and threshold voltage shift of the floating gate (gate 1). The threshold voltage shift ΔV_{th} is limited by the gate2 bias as shown in Fig.5. This limitation will be due to the decrease of the oxide field by the charged floating gate. Considering application to an imaging device , the threshold shift ΔV_{th} vs. illumination intensity was measured with exposure time of 1 min.. Linear relationship in Fig.6 suggests possibility of gray scale detection. As shown in Fig.3, a tranparent electrode (floating gate) is composed of two sets of

thickness combination of SiO_2 and poly-silicon disposed side by side and has two complementary interference color (green and red) in the respective position. Relatively flat wave length response is observed ranging from the wave length of 3300 Å to infrared.

CONCLUSION and DISCUSSION

A novel non-volatile optical memory for visible and infrared light was proposed and fabricated. The device was electrically erasable. Theoretical explanation on the charging time constant was reasonably made. The time constant was of the order of second, but this can be greatly shortened by surface doping of the substrate. The shallow surface doping easily reduces d to 1/2 or 1/3 of the present value ,resulting decades of improvement in d. In this case, surface depletion layer width remain relatively unchanged under the same bias, V_{DB} and is effective for the detection of long wave length light.

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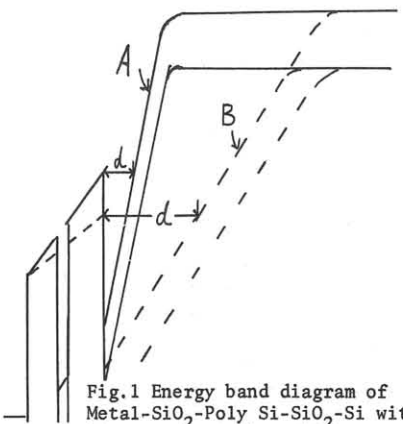

Fig.1 Energy band diagram of Metal-SiO_2-Poly Si-SiO_2-Si with bias; curve A shows higher electricfield near surface drain-substrate junction than curve B.

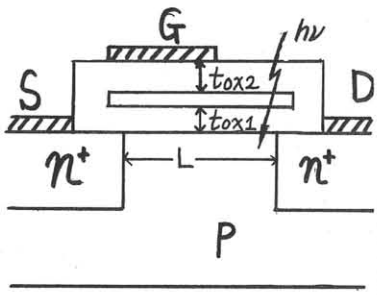

Fig.2 Transparent poly-Si floating gate FET
L = 40 μ, W = 35 μ,
t_{ox1} = 500 Å, t_{ox2} ≃ 1000 Å

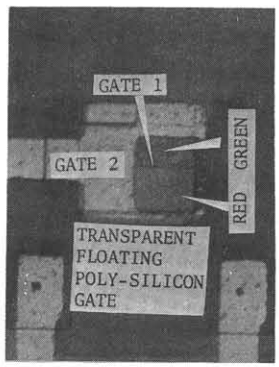

Fig.3 Micro-photograph of the experimentally fabricated n-channel device.

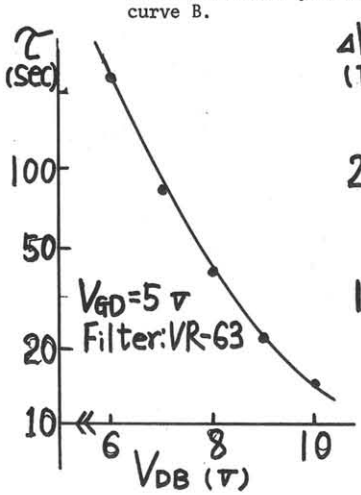

Fig.4. Charging time constant vs. drain bias V_{DB} under tungsten lamp illumination through color filter VR-63.

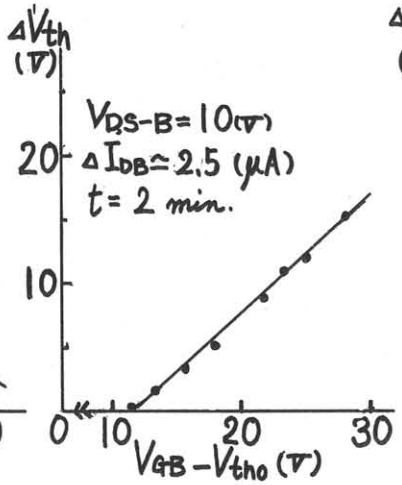

Fig.5 Threshold voltage shift V_{th} vs. gate voltage V_{GB} .

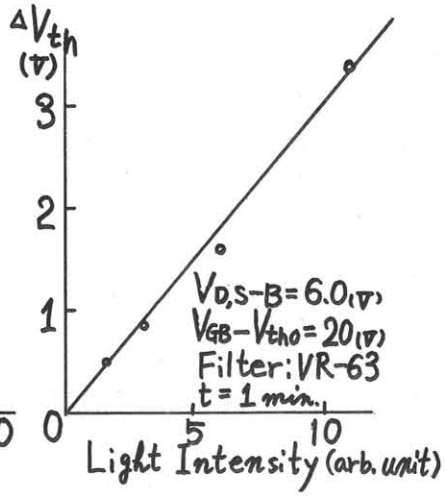

Fig.6 Threshold voltage shift V_{th} vs. light intensity.

References
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(2) R. J. Powell; J. of Appl. Phys., vol.41, No.6,pp.2424 -2432, May,1970.
(3) D. J. Bartelink et al; Phys. Rev.,vol.130, pp.972 - 985, May 1, 1963.