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INVITED: THE BUCKET BRIGADE AND OTHER CHARGE TRANSFER DEVICES

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Some important factors which characterize the performance of charge transfer devices in analog applications are:

1. charge transfer inefficiency as a function of clock frequency.
2. signal-to-noise ratio (dynamic range).
3. influence of leakage current and surface state loss on dynamic range.

The transport of charge in a bucket brigade and in a charge coupled device with electrode lengths of 10 μm or more is effectuated by self-induced drift and by diffusion. Both devices exhibit the same maximum clock rate for comparable geometrical dimensions.

At low clock rates the charge transfer inefficiency in a BB is limited by drain-to-source feedback. Owing to this effect the channel length of the MOS transistors cannot be chosen smaller than about 5 μm. Due to the influence of parasitic gate overlap capacitance and substrate capacitance the storage capacitance has to be at least a factor of 2 larger than the gate capacitance. These geometrical limitations result in a rather low maximum clock frequency for the Al-gate MOS BB (charge transfer inefficiency of 2.10^{-3} at a clock rate of 0.5 MHz).

The MOS tetrode configuration offers a possibility of reducing the feedback effect with a factor of 10 or more. This has been experimentally verified in an audio delay line with 512 BB stages on one chip.

A second method of reducing feedback in a BB is the application of a varactor-type storage capacitance, such as the capacitance of an inversion-layer.

If the value of the storage capacitance is reduced from C_{st} to a much smaller value of C_{res} during each transfer process, the feedback is reduced with a factor of C_{res}/C_{st}. In addition this procedure results in a faster transfer of the last fraction of the signal charge and in a reduction of the transfer process noise.

A varacter BB fabricated with p-channel LOCOS silicon gate technology promises a charge transfer inefficiency of 2.10^{-4} at 1 MHz clock rate. This speed limit can be increased with a factor of 3 by applying trapezoidal clock pulses. The use of double-diffused MOS structures possibly leads to a further improvement in speed performance.

In a CCD in principle all mobile charge is transferred; a voltage feedback will not result in a modulation of the remaining charge and has no influence on the signal. At low clock frequencies the charge transfer inefficiency in a surface CCD is limited only by surface states. The charge transfer in a CCD with small electrode lengths on a lightly doped substrate is improved significantly by fringing fields. Maximum clock rates of 100 MHz have been predicted for these devices.

The most promising CTD concept, especially for imaging applications, seems to be a CCD with transport of majority carriers in the bulk, because in this device the influence of fringing fields on the last fraction of the signal charge is much larger than in a surface CCD due to "capacitive decoupling"[1]. An experimental device realised in our laboratories based on this principle shows a charge transfer inefficiency of less than 10^{-4} at clock rates in excess of 100 MHz.

1. L.J.M. Esser: "Peristaltic CCD", Electronics Letters 8 (1972), 620.