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An Improved Self-Scanned Linear Photosensor Array

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A present-day self-scanned photodiode array usually consists of photodiodes, switching MOSTs and a shift register. The maximum clock rate of the shift register primarily limits the array performance relating to the scanning speed. To the author's knowledge, the highest clock rate achieved is around 3 MHz. There has been developed some sophisticated technique using the overlapped shift pulse method[1] to overcome the above limit and the effective scanning speed as high as 10 MHz/bit has been reached in the array. Yet there remains the stromg demand for the higher speed scanning circuitry in order to extend the application field of the solid state imager.

In MOST shift registers for scanner use, a pair of inverters are normally used, irrespective of the number of the unit circuit consisting MOSTs. Moreover the operational noise margin of the inverter requires the design of the different g_m ratio between the load and the driver. Along with the need for the smallest possible layout area, this leads to the smaller g_m of the load MOST, which results in the slower rise time of the output pulse. Twice of the rise time determine the maximum clock rate. Fig.1 shows a diagram of the newly designed circuitry for a linear sensor array. One stage of the scanner consists of a new ratioless-type and a ratio-type inverter. The former has three MOSTs Q_1, Q_2, Q_3 for which any deisgn consideration on g_m ratio is not necessary. They play a role of transfer gate, memory and charge-discharge respectively. With this ratioless inverter, the scanner is proved to be twice faster than the conventional one. Shown in Fig.2, is the measured frequency

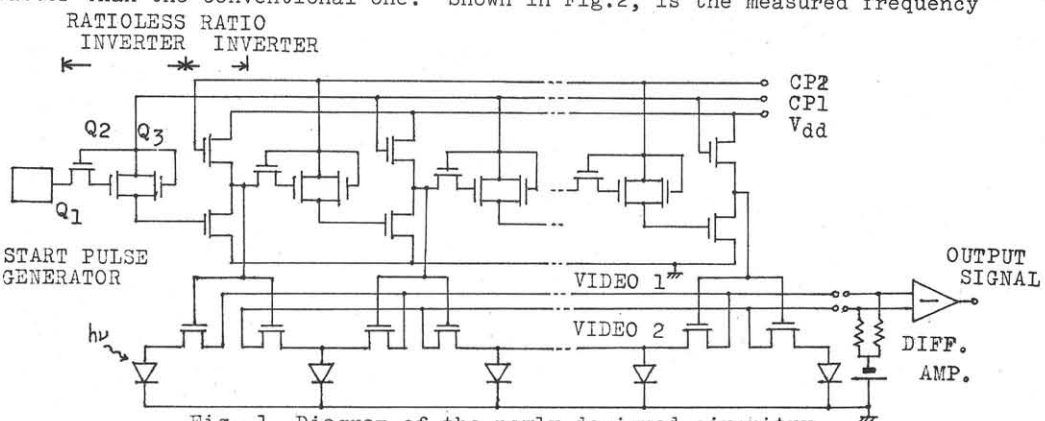

Fig. 1 Diagram of the newly designed circuitry for a linear sensor array

characteristics of the scanner, which can operate beyond 5 MHz. Besides, the new scanner ensures a high operational noise margin, as the on-level of the inverter reaches completely to the earth level. Moreover, the occupied area of a single stage is easily diminished down to a half that of the conventional scanner, which promises the higher resolution capability of the array.

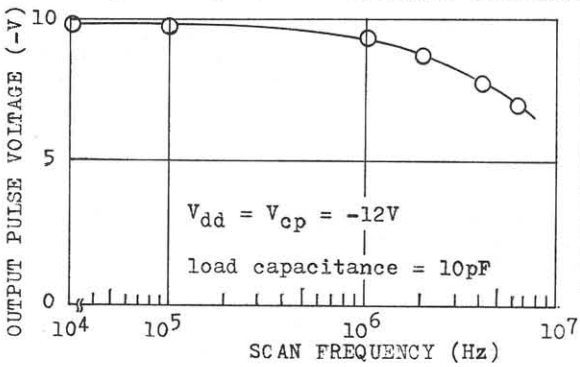

Fig. 2 Frequency dependence of the output pulse voltage

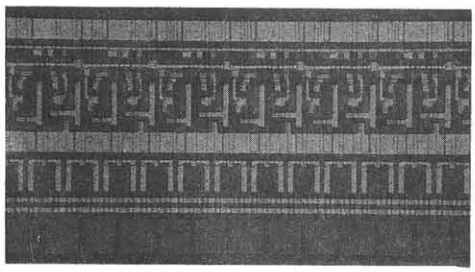

Fig. 3 Photograph of a portion of the developmental 256-bit photosensor array

A start pulse generator consisting of several MOST logic circuit is integrated on the same chip, for the purpose of avoiding the rather complicated circuitry outside the chip. The spike noise inherent in these solid state imager is cancelled out by the neighboring-bit correlation technique.(2)

Fig.3 is a portion of a photomicrograph of the developmental 256 bit array fabricated by the conventional MOS processing technology. As an example of the gray-scale reproduction capability, a picture taken with the array is shown in Fig.4.

A self-scanned linear photosensor array having a high speed scanning circuit, together with the noise cancellation technique and with a start pulse generater, is designed and fabricated successfully to be proved to show an excellent analogue performances over the conventional one. This promises a concrete step forward to the solid state imager replacing the pick-up tubes.

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Fig. 4 Picture taken with the array

References

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(2) M. Ashikawa etal; "A New Spike Noise Elimination Technique for Photosensitive Arrays", ISSCC Digest of Technical Papers,p.129, 1973