INTRODUCTION

IMPATT diodes have shown their excellency in the microwave frequency range higher than attained by the other devices of the same dimension and material. But they were two terminal devices and require additional circuit techniques and components to use as amplifiers. On the other hand, to attain high frequency amplification, an IGFET has obstacles such as increase of input and output loss in microwave frequency range and drain to gate feed back capacitance. With insulated gate controlling carriers transiting with saturation velocity, IMPATT diodes will find their undeveloped application and remove obstacles with an IGFET.

DEVICE STRUCTURES and FIRST ORDER ANALYSIS

Figs. 1, 2 and 3 show device structures proposed and experimentally fabricated. A non-planar type device can offer a small input time constant and small feedback capacitance but suffers from high output capacitance. A planar type device can realize small output capacitance but fine pattern technology is required to reduce its input time constant.

A simplified structure for a first order estimation of the device characteristics is shown in Fig. 4. Gate field, $E_G$ in semiconductor is given by

$$E_G = V_G / (t + t_I E_se / E_L) \quad \cdots \quad (1)$$

where $t$ and $t_I$ denotes length of line of force of gate field in semiconductor and gate insulator, and $E_se$ and $E_L$ is dielectric constant of the semiconductor and gate insulator. $V_G$ is gate to source voltage. This field $E_G$ is added to drain field, $E_D$

$$E_D = V_D / L \quad \cdots \quad (2)$$

to control the avalanche breakdown in avalanche region under gate. Assuming following relation between ionization coefficient, and electric field $E$ as eq. (3),

$$\alpha = \alpha_o \exp - b (E_o / E)^m \quad \cdots \quad (3)$$

static characteristics at low level current can be expressed as,

$$J = J_s \left[ 1 - \int \alpha \, dx \right]^{-1} \quad \cdots \quad (4)$$

$$J \propto J_s \left[ 1 - \alpha_o \int \exp - b (E_o / E_G + E_D)^m - \alpha_o L_D \exp - b (E_o / E_D)^m \right]^{-1} \quad \cdots \quad (5)$$

In the above equation, carriers are assumed for the simplicity to transist in the avalanche region nearly along the quarter circular trajectory shown by a dotted line in Fig. 4 and turn to a straight trajectory to low resistive drain. $t$ increases up to nearly $E_L / E_G$ as the gate bias $V_G$ increases. Static voltage gain, $A = V_D / V_G | I_D |$ const. reduces as $V_G$ increases. A device with $t_I = 1000 \AA$ and drain to source length, $L = 3$ will show voltage gain of about 30 at low gate bias ($V_G \approx 25$).

Small signal parameters will reflect the delay and negative resistance in the avalanche region and the transit delay of the drift region.

EXPERIMENTAL RESULTS

Devices shown in Figs. 1, 2 and 3 are experimentally fabricated. Fig. 5 shows static characteristics of a planar type transistor. Static voltage gain is realized as predicted by a simple theory. Break down voltage showed initial "walk-out" due to charging of carrier charge into traps in the gate oxide. This charging effect was not observed in pulsed avalanche breakdown of MOS diodes made by the same oxidation and metallization process with the device. This indicates that one of the origins of the traps in the devices' oxide may be strain caused by impurity diffusion or oxide step between thick and thin oxide. Trap free oxide process throughout fabrication processes should be developed to reduce the walk-out of the breakdown voltage.
Measured small signal parameters of a non-planar type device shows characteristic features in $Y_{11r}$ and $Y_{22r}$ as shown in Figs.6 and 8. For instance, they decrease as signal frequency increases. This tendency can be explained by a inductive component in the avalanche region. In case of a conventional IGFET these parameters increases as the signal frequency increases. As shown in Fig.7, power gain is calculated as 7dB at 2GHz from measured s-parameters and the experimental device shows relatively high gain under the low current bias of $I_D=0.5mA$.

CONCLUSION and ACKNOWLEDGEMENT

A new device, Insulated Gate Avalanche Transistor (IGAT) was proposed and experimentally fabricated. The device showed reasonable gain in the GHz frequency range. The walk-out of breakdown voltage was left to await trap free oxide process. Control of negative resistance of IMPATT mode by gate electrode will be expected.

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Fig.1 Planar type IGAT.
Fig.2 Non-planar type IGAT Fig.5 A static characteristics of a non-planar type IGAT. ( $I_s=3uA$, $L_s=4uA$, $t_f=900A$ )
Fig.3 Micro-photograph of an experimentally fabricated non-planar type IGAT.
Fig.4 A model of IGAT for analysis.
Fig.6 Y-parameters vs. frequency of a non-planar type IGAT. ( $I_s=1.5uA$, $L_s=1500A$ )
Fig.7 Maximum stable power gain of a planar and non-planar type IGAT.
Fig.8 Current dependence of measured $y$-parameters of a non-planar IGAT.

REFERENCE