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INSULATED GATE AVALANCHE TRANSISTOR

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INTRODUCTION

IMPATT diodes[1] have shown their excellency in the microwave frequency range higher than attained by the other devices of the same dimension and material. But they were two terminal devices and require additional circuit techniques and components to use as amplifiers. On the other hand, to attain high frequency amplification, an IGFET has obstacles such as increase of input and output loss in microwave frequency range and drain to gate feed back capacitance.[2] With insulated gate controling carriers trasitting with saturation velocity, IMPATT diodes will find their undeveloped application and remove obstacles with an IGFET.

DEVICE STRUCTURES and FIRST ORDER ANALYSIS

Figs. 1,2 and 3 show device structures proposed and experimentally fabricated. A non-planar type device can offer a small input time constant and small feed-back capacitance but suffers from high output capacitance. A planar type device can realize small output capacitance but fine patterning technology is required to reduce it's input time constant.

A simplified structure for a first order estimation of the device characteristics is shown in Fig. 4. Gate field, E_G in semiconductor is given by

$$E_G = V_G/(t + t_I \varepsilon_{se}/\varepsilon_I) \quad \cdots\cdots (1)$$

where, t and t_I denotes length of line of force of gate field in semiconductor and gate insulator, and ε_{se} and ε_I is dielectric constant of the semiconductor and gate insulator. V_G is gate to source voltage. This field E_G is added to drain field, E_D

$$E_D = V_D/L \quad \cdots\cdots (2)$$

to control the avalanche breakdown in avalanche region under gate. Assuming following relation between ionization coefficient, and electric field E as eq.(3),

$$\alpha = \alpha_0 \exp -b\,(E_0/E)^m \quad \cdots\cdots (3)$$

static characteristics at low level current can be expressed as,

$$J = J_S\,[\,1 - \int \alpha\, dx\,]^{-1} \quad \cdots\cdots (4)$$

$$J \simeq J_S\,[\,1 - \alpha_0 t \exp -b\{E_0/(E_G + E_D)\}^m - \alpha_0 L_D \exp -b(E_0/E_D)^m\,]^{-1} \quad \cdots\cdots (5)$$

In the above equation, carriers are assumed for the simplisity to transit in the avalanche region nearly along the quarter circular trajectory shown by a dotted line in Fig.4 and turn to a straight trajectory to low resistive drain. t increases up to nearly $\frac{\pi}{2} L_G$ as the gate bias V_G increases. Static voltage gain, $A = V_D/V_G|_{I_D = \text{const.}}$ reduces as V_G increases. A device with t_I=1000Å and drain to source length, L=3 will show voltage gain of about 30 at low gate bias ($V_G \gtrsim 25$).

Small signal parameters will reflect the delay and negative resistance in the avalanche region and the transit delay of the drift region.

EXPERIMENTAL RESULTS

Devices shown in Figs.1,2 and 3 are experimentally fabricated. Fig.5 shows static characteristics of a planar type transistor. Static voltage gain is realized as predicted by a simple theory. Break down voltage showed initial "walk-out" due to charging of carrier charge into traps in the gate oxide. This charging effect was not observed in pulsed avalanche breakdown of MOS diodes made by the same oxidation and metalization process with the device. This indicates that one of the origins of this traps in the devices' oxide may be strain caused by impurity diffusion or oxide step between thick and thin oxide. Trap free oxide process throughout fabrication processes should be developed to reduce the walk-out of the breakdown voltage.

Measured small signal parameters of a non-planar type device shows characteristic features in Y_{11r} and Y_{22r} as shown in Figs.6 and 8. For instance, they decrease as signal frequency increases. This tendency can be explained by a inductive component in the avalanche region. In case of a conventional IGFET these parameters increases as the signal frequency increases. As shown in Fig.7, power gain is calculated as 7dB at 2GHz from measured s-parameters and the experimental device shows relatively high gain under the low current bias of I_D=0.5mA.

CONCLUSION and ACKOWLEDGEMENT

A new device, Insulated Gate Avalanche Transistor (IGAT) was proposed and experimentally fabricated. The device showed reasonable gain in the GHz frequency range. The walk-out of breakdown voltage was left to await trap free oxide process. Control of negative resistance of IMPATT mode by gate electrode will be expected.

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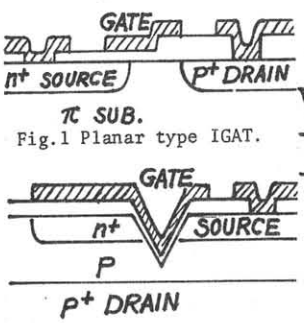


Fig.1 Planar type IGAT.

Fig.2 Non-planar type IGAT.

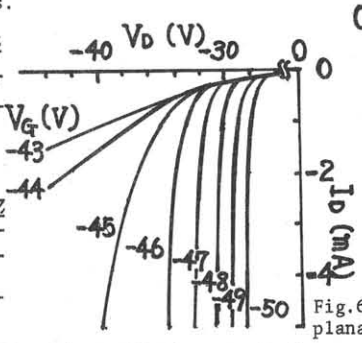


Fig.5 A static characteristics of a non-planar type IGAT. (L≃3μ, L_G≃2μ, t_I≃900Å)

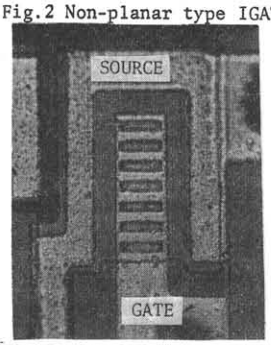


Fig.3 Micro-photograph of an experimentally fabricated non-planar type IGAT.

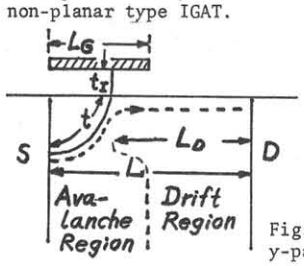


Fig.4 A model of IGAT for analysis.

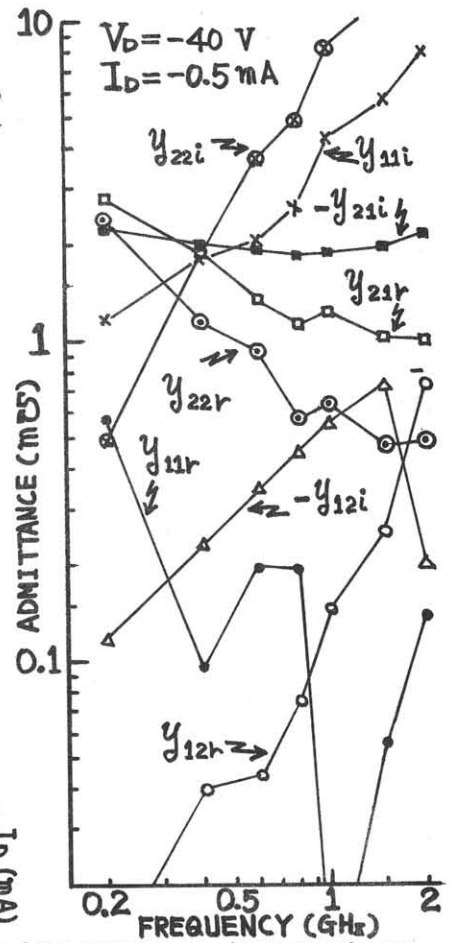
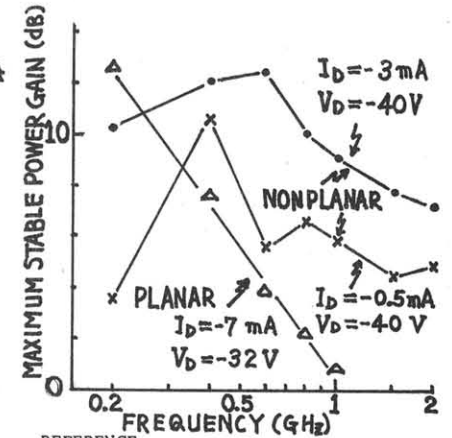


Fig.6 Y-parameters vs. frequency of a non-planar type IGAT. (L≃1.3μ, L_G≃1μ, t_I=1500Å)

Fig.7 Maximum stable power gain of a planar and non-planar type IGAT.



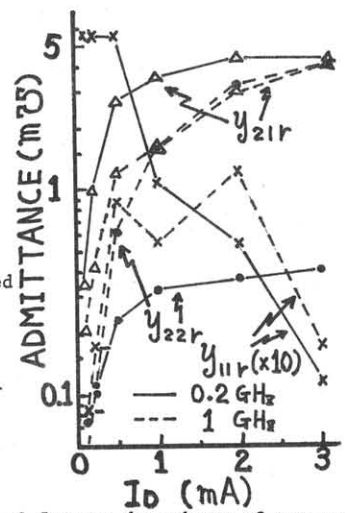


Fig.8 Current dependence of measured y-parameters of a non-planar IGAT.

REFERENCE

(1) T.Misawa,"IMPATT diodes", Semiconductor and Semimetals, vol.7, chap.7.

(2) Y.Hayashi and Y.Tarui,"DSA-MOS transistor (VII)",1971 National Convention of IECE of Japan,913 (in Japanese)