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Single- and Dual-Gate GaAs Schottky Barrier FET's for Microwave Frequencies

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The GaAs Schottky barrier gate FET has opened a new era of microwave transistors by extending the frequency range of low-noise, solid-state amplification up to 10 GHz. The best result reported so far is a cutoff frequency of around 50 GHz with a 1 μ-gate device directly mounted on a stripline circuit.[1,2] By improving the design and process technology, we have realized this highest cutoff frequency with a gate length of 1.5 μ. Furthermore, in order to increase flexibility of the GaAs FET, a dual-gate device has been designed and fabricated. These devices are conveniently mounted in small-size ceramic packages.

The GaAs FET's were fabricated using n-type epitaxial layers, with carrier concentration of 4 - 7 x 10^{16} cm^{-3} and thickness of 0.2 - 0.4 μ, grown on Cr-doped high-resistivity substrates. The vapor-phase etching and EDTA treatment were found to be important to improve the quality of thin epitaxial crystals.[3] Source and drain were Au/Ge films evaporated and alloyed on an isolated mesa structure. The composition of the metal was chosen so as to minimize the contact resistance and the surface roughness caused by alloying. The gate was formed by successively evaporating Cr, Mo, and Au. Conventional contact photomasking and lifting process were used to delineate the metal electrodes.

With the electrode geometry (see Fig. 1) reasonably optimized on the basis of cut-and-try experiments, the single-gate FET was designed for optimal microwave performance by appropriately choosing the thickness of the active epitaxial layer. Figure 2 shows the unilateral gain and minimum noise figure of a 1.5 μ-gate GaAs FET contained in a package. The maximum frequency of oscillation was as high as 50 GHz. The noise figure was 2.9 dB at 4 GHz and increased only by 1 dB with an octave increase of frequency. These results are comparable to the best performance reported so far.

While the single-gate device is suitable for pursuing the high-frequency limits of the FET, the dual-gate version finds more versatile applications at comparatively low frequencies.[4] A simple design theory of the dual-gate FET was worked out based on the model of two cascode-connected common-source and common-gate FET's. Samples were fabricated in a way similar to the single-gate devices. The noise figure and power gain measured at several frequencies (see

Table I) compare much favorably with those of conventional Si MOS counterparts, and demonstrate the usefulness of GaAs dual-gate FET's at microwave frequencies. The gate-bias dependence of unilateral transducer gain G_{max} (see Fig. 3) illustrates one of the attractive functions of the tetrode FET, i.e., automatic gain control by means of 2nd-gate bias. Another benefit of the dual-gate structure is a reduced feedback, or the resulting improvement of gain and stability. The stability factor and maximum stable gain were several times larger, but the available gain was comparable or lower for the dual-gate FET as compared to the device with a single gate of the same dimensions with the first gate of the former.

Since our single- and dual-gate FET's are both mounted in packages with diameters of only 1.8 mm (see Fig. 4), they can be characterized individually and readily incorporated in microstripline amplifier circuits.

1) W. Baechtold, IEEE J. Solid-State Circuits SC-8, No.1, 54 (1973)

2) C. A. Liechti et al., Digest of Technical Papers, ISSCC'73, p. 74

3) S. Asai et al., Proc. 4th Conf. on Solid-State Devices (Tokyo, 1972) p. 71

4) J. A. Turner and S. Arnold, Microwaves 11, No.4, 44 (1972)

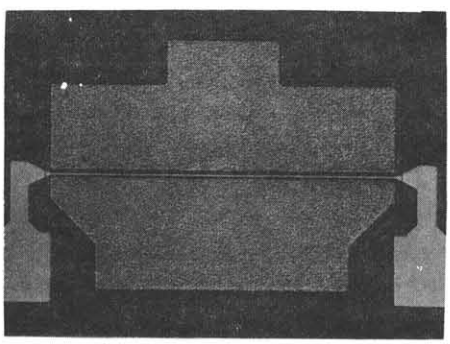

Fig. 1

Table I

SAMPLE	FREQ (GHz)	opt. PG		opt. NF	
		PG(dB)	NF(dB)	PG(dB)	NF(dB)
1	0.8	19.0	3.7	17.2	2.9
2	1.7	10.5	4.1	10.0	3.6
3	4.0	11.1	5.5	9.8	4.7

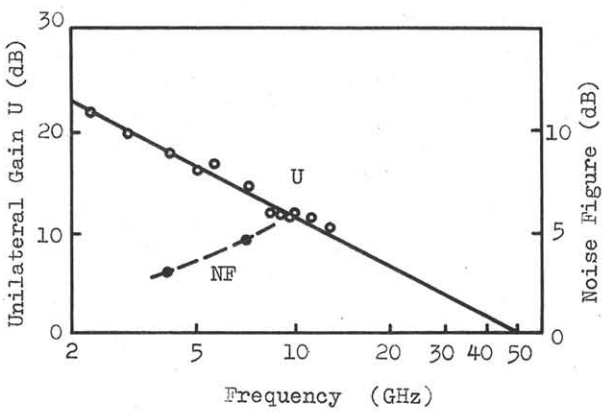

Fig. 2

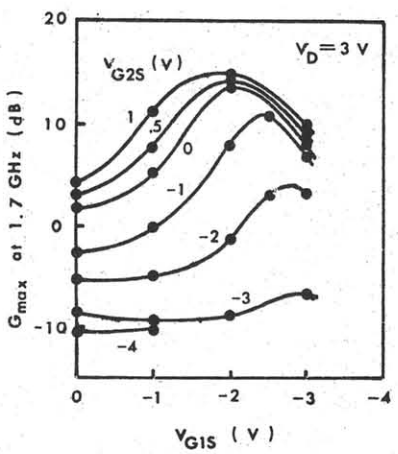

Fig. 3

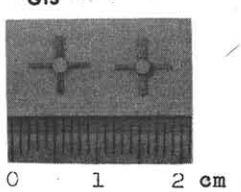

Fig. 4