8-9 Design, Fabrication and Characterization of a Double Emitter Phototransistor Array for Optical Memory System

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Double emitter phototransistor arrays have advantages in ease of fabrication and operation. They are analyzed thoroughly for readers for high capacity digital optical memory. New operation modes are proposed.

Structure and schematic diagram of charge storage mode of double emitter phototransistor are shown in Fig.1. The large emitter E2 serves to select word line and also as a cross-under at the intersection of E1 and E2 lines. The period $t_2 \sim t_3$ is photon integration time.

For image sensor, Weimer operated double emitter phototransistor arrays by driving E1 and E2 with pulses and sensing output signal at common collector[1]. For optical memory, to save readout time and to reduce switching noises we used a new method that common collector is DC biased, read pulse is applied to E2 and the output signal is sensed from E1 lines simultaneously.

For digital use, the saturation point of input photon/output signal characteristics is important parameter (cf. Fig.2). Charge storage mode of the phototransistor means charge-discharge cycle of B-C and B-E2 junction. Collector is DC biased, the maximum storable charge is $C_{E2} \cdot V_{E2} (= \eta \cdot q \cdot N_{psat})$ where V_{E2} is read pulse voltage. Assuming an ideal diode for each junction and driving E2 with step pulse, the signal output is approximately given by following equation.

$$V_{out} = \frac{\eta \cdot q \cdot N_p}{C_C + C_{E2}} - \frac{C_C + C_{E2} + C_{E1}}{C_C + C_{E2}} \cdot V_D$$

where η is quatum efficiency, N_p is incident photon numbers, V_D is the voltage sufficient to forward-bias the base-emitter junction and C's are junction capacity.

For practical design, saturation output signal and photon number N_{psat} was computed by electronic computer as a function of device parameters. In these analysis, we consider characteristics of C-B-E1 transistor and the voltage dependence of each junction capacity.

The time constant of diffused E2 cross-under is 40~50 nano sec for 18 cells. To avoid dispersion of output signal level and delay, ramp waveform is used for read pulse. These time constant will be decreased by metal-metal cross-over. Output characteristics of the phototransistor are shown in Fig.2 for ramp drive pulse. Theoretical calculations closely agree with measured values. This enables optimization of double emitter phototransistor design for a particular set of requirments.

A photodetector that consists of four chips is fabricated. A chip contains

17x18 phototransistors which have 110 $\mu\phi$ photosensitive area, 50x40 μ^2 E2, 30 $\mu\phi$ E1 and 350 μ cell spacing. Fig.3 shows an example of waveform traces of the output signals and noises of 306 phototransistors (one chip).

Fig.4 shows the behavior of base potential corresponding to two incident photons. The signal output is not produced until the base-E1 junction becomes forward-bias. The smaller the incident photons, the longer the delay T_d and the shorter the signal width T_s. As T_d or T_s is easily converted to pulse width, the incident photon number is detected as pulse width modulated signal. When staircase waveform is applied to E2 as read pulse, the incident photon number detected as pulse number modulated signal as shown in Fig.5.

Analysis of double emitter phototransistor is carried out quantitatively. The results enable optimum design of double emitter phototransistor for practical requirments including driving metod. Some interesting modes of operation of phototransistor are described.

Reference 1) P.K.Weimer, F.V.Shallcross and V.L.Franz; IEEE J.Solid State Circuits SC-6,135(1971)

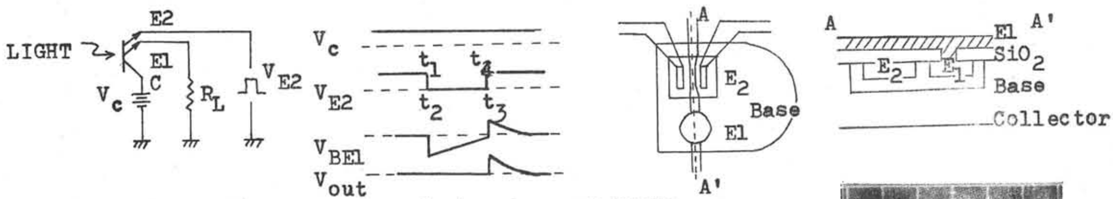

Fig.1 Charge storage mode and structure of DEPTR

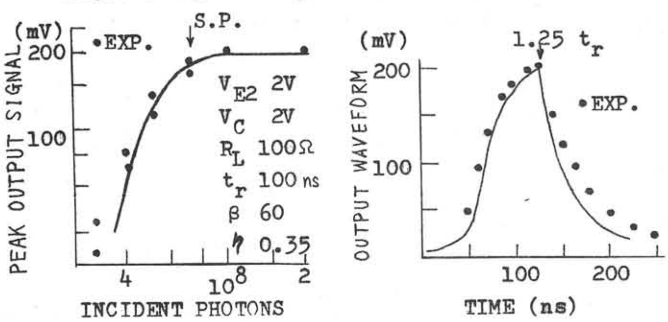

Fig.2 Output characteristics of DEPTR

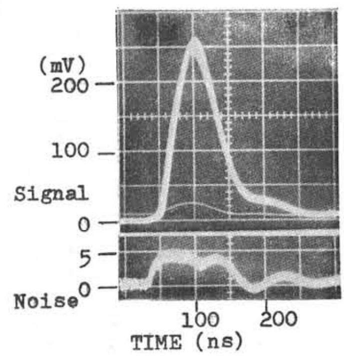

Fig.3 Waveform traces

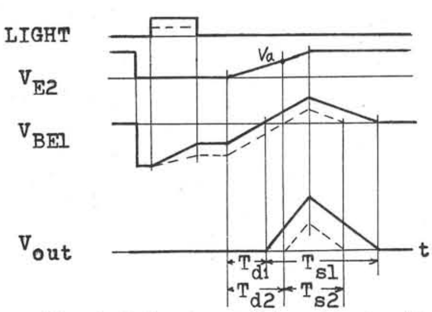

Fig.4 Behavior of base potential

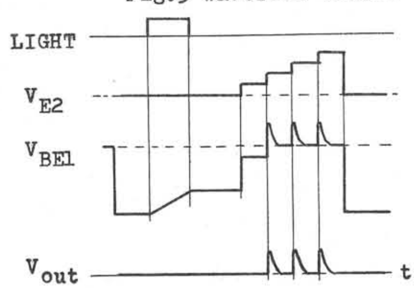

Fig.5 An example of pulse number modulated signal obtained by applying staircase waveform to E2