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A Novel Planar Multilevel Interconnection Technology Utilizing Polyimide

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ABSTRACT

A completely new planar method permitting step-free multilevel interconnections is proposed. The key role in this technique is played by the polyimide film which is used as insulating layers. The fluid property of the polymer solution always gives an ideal flatness to the surface of the wafer no matter how many steps are formed by preceding metallization processes. Using this planar metallization with polymer (PMP) technique, a five-level structure which consists of five metal (aluminum) and five polyimide layers has been successfully made. The PMP structure completely eliminates the failures which result from open circuits between metal layers at crossovers and via-holes and from short circuits between metal layers through the pin-holes of insulating layers. No trace of degradation is observed in the characteristics of the MOS-FET covered with the polyimide either after heating at 150°C for 2000 hours or after a bias-temperature test at 125°C for 200 hours. The polyimide used to this technique has been specially synthesized for semiconductor devices. Metal impurities such as sodium contained in the polyimide are smaller in quantity than that of silicon dioxide conventionally formed by chemical vapor deposition. Adhesive strength between silicon dioxide and the polyimide film is strong in the peeling test and kept the initial strength in the pressure cooker test for more than 32 hours. Further, adhesive strength between the metal film such as aluminum and the polyimide is also strong in the above tests. The PMP is also reliable as the mechanical structure. This PMP technology utilizing polymide is not only applied to the multilevel interconnections on LSI's but also applied to many semiconductor devices such as transistors, MOS-IC's and power IC's.