Digest of Tech. Papers The 6th Conf. on Solid State Devices, Tokyo, Sep. 1974

B2-3 IPOS Scheme : A New Isolation Technique for Integrated Circuits

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The great majority of bipolar integrated circuits have been formed using the P-N junction isolation technique. Many improved isolation technique have been developed to replace the conventional P-N junction isolation for increasing switching speed and the circuit packing density. However, their fabrication processes are rather complicated. In this paper, a new isolation technique named IPOS (Insulation by Oxidized Porous Silicon) that offers large circuit packing density, low parastic capacitances and high inter-device breakdown voltages is discussed with its application to integrated circuits.

1. Isolation Procedure

The anodic behavior of silicon electrodes in hydroflouric acid solution has already been investigated by Turner[1] et al. They have shown that thick porous films are formed below a critical current density. Our new IPOS scheme is based on this phenomenon[2]. In Fig.1, two basic IPOS procedures are shown. In procedure (a), P-type layers are selectively diffused through the N-type epitaxial layer to contact the P-type substrate, and then silicon slice is anodically polarized in concentrated hydroflouric acid solution. The rate of reaction for P-type silicon is much larger than that for N-type silicon, so only the P-type regions are anodized without any masking pattern. In (b), N-type epitaxial layer, covered with a pattern of silicon nitride, is directly anodized under illuminated condition. The uncovered regions are anodized selectively. These anodic porous films are very reactive and unstable, so thick insulating films are obtained by oxidizing then thermally for very short time. For example, oxidized porous silicon films of 5 μm thickness are obtained by oxidization at 1150 °C for 10 min in steam. While it takes about 35 hours at 1150 °C to get a silicon dioxide films of the same thickness by direct oxidization

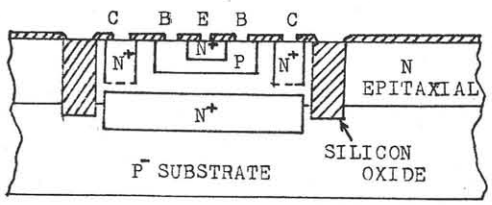

Fig.2

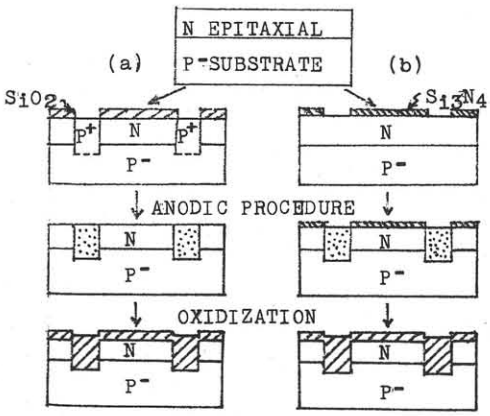

Fig.1

of bulk silicon. The transistor structure formed by IPOS is shown in Fig.2.

2. Isolation Characteristics

Fig.3 shows the isolation capacitance for both conventional P-N junction isolation and IPOS with the same structure of 47 by 52 μms bottom area and 4 μm thickness of epitaxial layer. This indicates that the IPOS scheme improves the isolation capacitance by a factor of 3 at a reverse bias of 10 volts. The capacitance for the IPOS structure is substantially equal to the capacitance of the bottom area. A inter-device breakdown characteristic of the IPOS structure is shown in Fig.4. The leakage current at a reverse bias of 20 volts is in the 10^{-7}-ampere range and the breakdown voltage is about 130 volts.

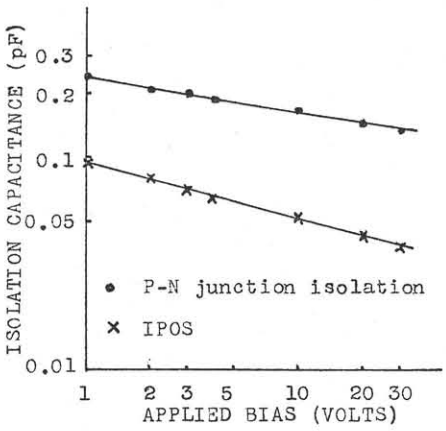

Fig.3

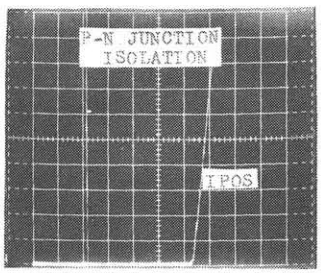

Fig.4 V:10μA/div H:20 V/div

3. Application to Integrated Circuits

Several types of logic gates were formed using the IPOS scheme. A circuit diagram of two-stage NTL gates with emitter followers is shown in Fig.5. A picture of its finished chip and a switching characteristic are shown in Fig.6 and Fig.7 respectivery. The f_T of the integrated transistor with a 2 by 25 μms emitter and double base stripes is about 6.5 GHz at a collector current of 10 mA and its base resistance is 30 Ω. A propagation delay of 0.31 nS/gate is obtained at a power dissipation of 24 mW/gate.

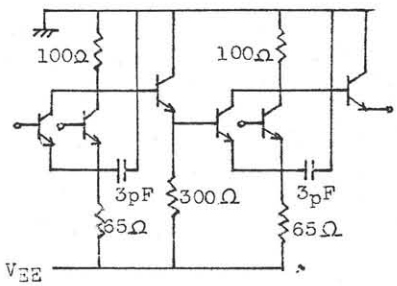

Fig.5

1)D.R.Turner,J.Electrochem.Soc.,105,402('58)
2)Y.Watanabe,T.Sakai,REVIEW of the ECL,19,899('71)

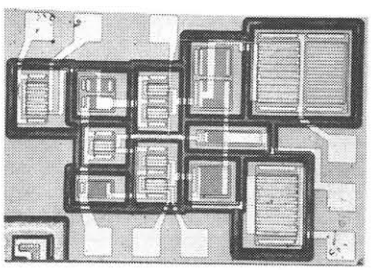

Fig.6

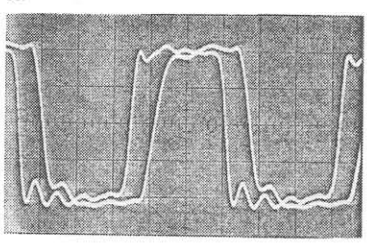

Fig.7 V:100mA/div H: 1 nS/div