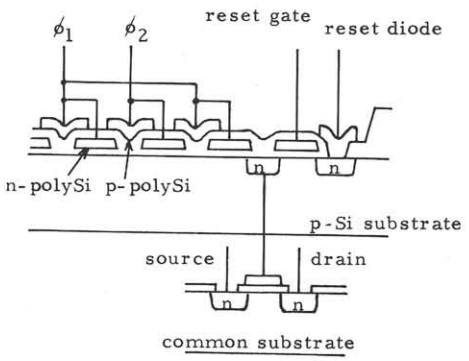
Digest of Tech. Papers The 6th Conf. on Solid State Devices, Tokyo, Sep. 1974

B4-2 An Improved Charge-Coupled Analog Delay Line

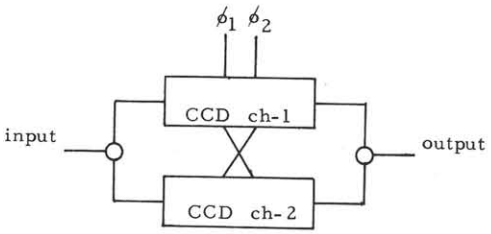
T. Sakaue, M. Iwasawa, Y. Horiike and K. Matsushima
Toshiba Research and Development Center
Tokyo Shibaura Electric Co., Ltd., Kawasaki

A new type charge-coupled device is presented for analog signal processing which offers many advantages in device characteristics. The structure of an n-channel, 64-bit device is shown in Fig. 1. The structure has two important features.

The first feature is an overlapping electrode structure in which both electrodes are of polycrystalline silicon but of opposite conduction types. As shown in Fig. 1(a), the conduction type of the first layer is opposite to that of the substrate, while the second layer is of the same type. Energy band diagrams for this structure are shown in Fig. 2. The contact potential difference is about 1 volt between the first layer and the substrate, and about 0 volts between the second layer and the substrate. As a result, a potential well corresponding to that difference in contact potential is already formed under the electrodes even with zero bias. Therefore, the device can be driven with lower clock voltages.



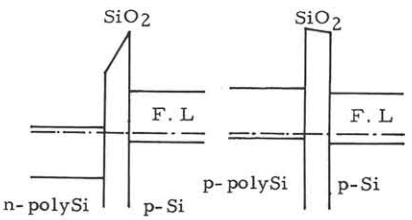
(a) Cross sectional view



(b) Double channel configuration

Fig. 1 Device structure

The second feature is a double channel structure consisting of two identical devices side-by-side with the connections to the first and second phases reversed, as shown in Fig. 1(b). Thus, data samples emerge alternately from the two channels at twice the clock frequency. The Nyquist limit, consequently, is increased by a factor of two. Moreover, because the last cells of the two CCD channels are driven with clock



(a) first layer (b) Second layer

Fig. 2 Energy band diagram

pulses of opposite phase, the spike noise from the clock pulses tends to be suppressed.

From the relation shown in Fig. 3(a) between the transfer inefficiency ϵ and the clock voltage V_{cp}, it is evident that the device operates well to voltages as low as 17 volts. Thus, compared to the conventional device with aluminum and poly-silicon electrodes, the present device requires three volts less clock voltage. As shown in Fig. 3(b), ϵ is less than 10^{-3} up to a frequency of 15 MHz, and thus the bandwidth of the device is also expected to be twice the usual Nyquist limit. The actual bandwidth is shown in Fig. 4 and is slightly less due to the limitations of the on-chip preamplifier. Finally, the great improvement in signal-to-noise ratio is shown in Fig. 5.

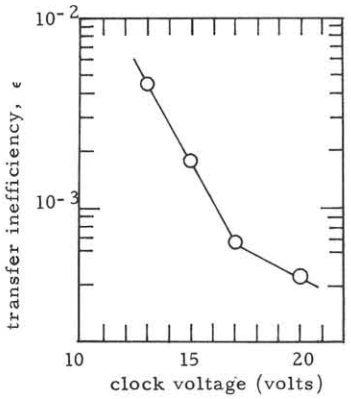


Fig. 3(a)

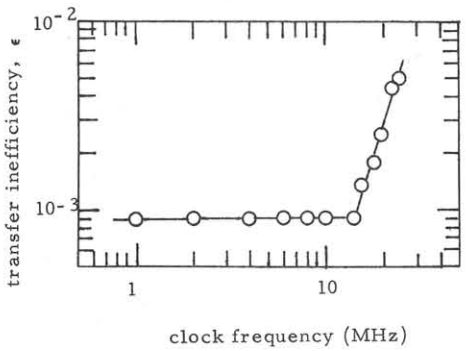
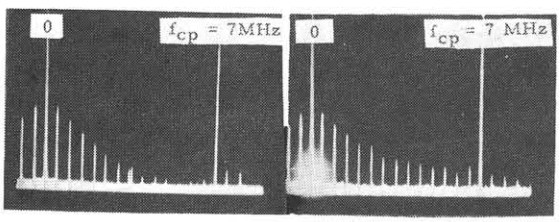


Fig. 3(b)



(a) (b)

Fig. 4 Frequency response characteristics

(a) single channel devices

(b) double channel devices

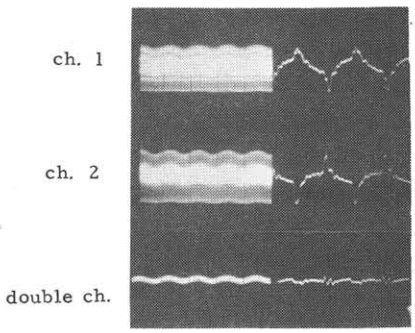


Fig. 5 Noise suppression

Using this improved CCD, delay of video signals has been demonstrated and the usefulness of the device in the field of video signal processing has been confirmed.

The authors are grateful to Mr. H. Saito and K. Terakawa for fabrication of the test devices and to Mr. M. Matono for the measurements.