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B4-3 Very High Speed, Clock-Pulse-Less Scanner for Solid State Imager

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Multi-phase clock pulses are believed to be indispensable for the operation of the shift register type scanner in MOS image sensor which has ever been made. However, the scanner suffers from the following two difficult problems; (i) lower S/N ratio due to the spike noise as the differentiated form of the clock pulses, (ii) limiting ability to follow the higher rate of the clock pulses. In this paper, we propose a novel very high speed scanner which can operate without the aid of the clock pulses. The performance of the developmental 670 bit linear sensor with the new scanner is also described.

Fig.1 shows the circuit configuration of the sensor where the unit stage of the scanner consists of a pair of inverters and a transfer gate. Only dc voltages are applied to the circuit. When the start pulse is introduced to the input inverter of the first stage, we obtain, at the node O_1, the first output V_{O1} having the waveform illustrated in the figure. The rise time is much slower, say 15 times, than the fall time, because of the larger g_m ratio between the driver and the load MOST, which is neccesary for proper operational margins. Neglecting the effect of the transfer gate, the next inverter turns on when V_{O1} just exceeds the threshold voltage. Accordingly, the scond output V_{O2} appears with the time delay t_d defined by the period between the onset of V_{O1} and the turn on of the inverter. A sequence of the same procedure throughout the scanner produces a series of the output pulses, delayed each other by t_d. These pulses open the switches to the photodiodes in the usual time sequential manner. The overlapping of the pulses gives no problem to the operation of the sensor, unless the read out time of the diode is not much longer than t_d.

Fig.2 represents an example of the computed waveforms of the three sequential output pulses for the case of the same -12 V applied to each line . The delay time

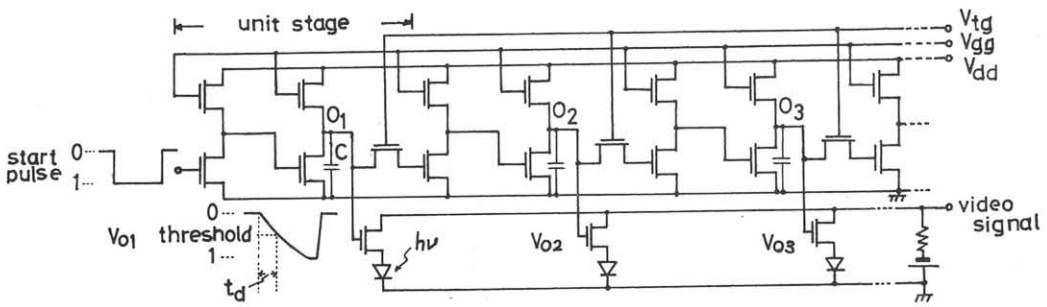


Fig.1 Circuit configuration of the sensor

is mainly determined by the ratio of the output capacity C to the g_m ratio of the load MOST, but can be varied or controlled by the applied dc voltage. The transfer gate plays some auxiliary role to widen the controllable range of the delay time. This intentional and controlled use of t_d for generating scan pulses makes a unique and excellent feature of our sensor.

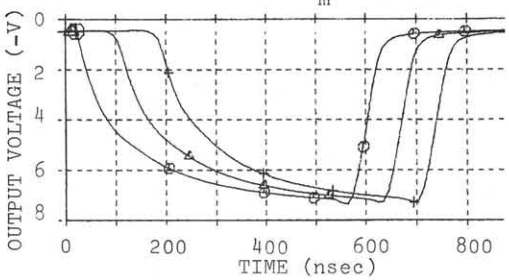


Fig.2 Sequential output pulses of the scanner

In Fig.3 is shown a photomicrograph of the experimentally fabricated sensor. The scanning speed is measured as a function of the voltage, V_{gg} and V_{tg}, and the result is illustrated in Fig.4. The curves clearly indicate that the scanning speed can be varied in the wider range, for example, from 10 to 30 MHz. This highest value, 30 MHz, far exceeds the speed of the conventional sensor (~10 MHz at most). The oscillograms of the output video signal taken with the scanning rate 10 and 20 MHz under the uniform illumination are shown in Fig.5. Because of the clock pulse less operation, the spike noise is reduced by two orders of magnitude compared to the conventional scanner and we can not recognize any noise in the picture.

As mentioned above, the novel features of high speed capability and excellent S/N ratio are proved by the experiment. And, moreover, a delay time control circuit is developed to assure the stable operation of the sensor under the practical conditions. The details of its operational characteristics will be presented at the conference.

The authors are grateful to Dr. M. Nagata for his helpful discussions.

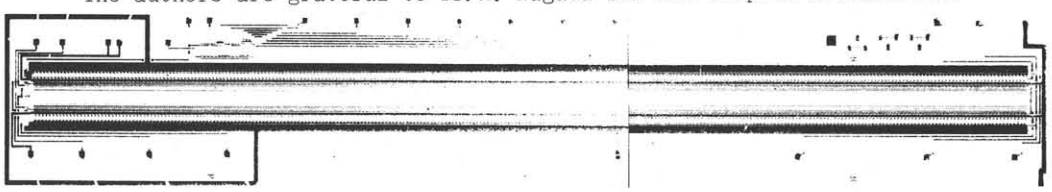


Fig.3 Photomicrograph of the developmental 670 bit image sensor

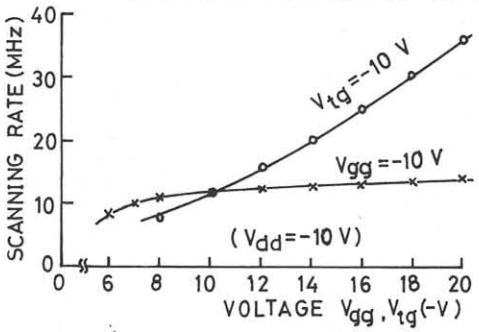
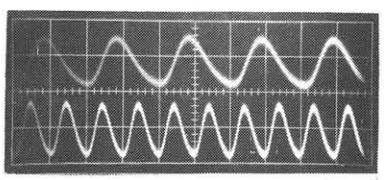


Fig.4 Scanning speed versus applied dc voltage



Hor. 50 nsec/div.
Ver. 20 mV/div.

Fig.5 Output video signal under uniform illumination