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B5-2 The Nature and Mechanism of Degradation in MNOS Read Write Memory

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I. Introduction

Degradation of MNOS memory transistor characteristics after a number of erasing/writing cycles has been investigated in connection with practical realization of non-volatile random access memory.[1],[2] General features are: (a) separation of the threshold voltages of "1" and "0" logic decreases with increasing cycles, (b) the center voltage of a hysteresis loop goes up slightly at first and then starts going down. The purpose of this paper is to describe a novel finding on the recovery of degraded MNOS memory as well as the physical aspects of mechanisms behind the phenomenon. We will also discuss the feasibility of fabricating a non-volatile random access memory without practical limitation to writing/erasing cycles.

II. Experimental

P-channel MNOS transistors were made by using the wellknown MOS techniques except for the ultra-thin oxide and nitride formations. Oxygen diluted with argon was introduced to a resistance heated tube furnace at 950°C to produce the 20 Å thick oxide with good reproducibility. A silicon nitride film of 500 Å was then deposited on the oxide by means of the chemical reaction of $SiHCl_3$ and NH_3 in a nitrogen ambient. The photolithgraphic length of the channel was 10 microns in each transistor and the p-n junction depth was 2 microns.

The erasing/writing characteristics were obtained for several combinations of pulse voltages and widthes using a minicomputer controlled testing system. The measurements of threshold voltages were carried out by applying a step-like pulse to the gate untill the drain current reached a certain amount, such as 1 microampere at the drain bias voltage of 5 volts.

III. Results and Discussion

The initial characteristics of the MNOS transistors were: (a) threshold voltage window is about 5 volts for pulse amplitudes of $\pm$ 33.5 volts and 5 microseconds pulse width, and the center voltage is about 2.5 volts, (b) surface mobility in the triode region is 270 $cm^2/v \cdot sec$ at room temperature, but sometimes it appears to be 120 to 170 $cm^2/v \cdot sec$, (c) surface state density is approximately 5×10^{12} $cm^{-2}eV^{-1}$, which has been determined by the temperature dependence of the threshold voltages, and (d) charge retention or , in other words, logarithmic rate of change of the threshold voltage is typically 200 to 300 mV/decade.

After applying write/erase pulses with various combinations of pulse amplitudes and widths, we measured the changes in the above characteristics which are: (a) the threshold window decreases monotonically with increasing cycles and the center voltage goes up slightly at first untill 10^{6-7} cycles. Then, the decrease in the window almost stops, while the center voltage starts going down untill 10^{8-9} cycles. When the pulse amplitude remains in a suitable range, a strange recovery phenomenon appears so that the center voltage tends to come back toward the initial state with increasing cycles.

(b) The mobility also decreases to 100 to 120 or even lower value, but it again recovers toward the initial value under the condition,,under which the center voltage comes up beyond 10^{8-9} cycles. These results are summarized in Fig.1. (c) The surface state density also behaves similarly to the mobility, i.e., monotonically increasing with the number of cycles untill 10^{8-9} and then decreasing. (d) The change in charge retention seems to support the prediction which is based on the model that the retention is governed by the back-tunneling process of electrons and/or holes from the traps in the nitride to the surface states at the silicon-silicon dioxde interface. Furthermore, we carefully measured the temperature dependence of the surface mobility as a function of gate fields at several write/erase cycles and found that the decrease in mobility would be explained by the Coulomb scattering process due to the ionized states as shown in Fig.2. This is also in consistence with the other facts.

The strange behaviors of a couple of quantities described here are quite sensitive to the pulse amplitude and width. Considering the similar measurements in the case of avalanche injection into the nitride, this is very important fact in designing a non-volatile random access memory, because the avalanche-tunneling mode[3] could be the only way to succeed in fabricating RAM without any rigorous restriction against bit isolations.

IV. Conclusion

Degradation in MNOS memory transistors has been studied after a number of erasing/writing cycles. With suitable combinations of electric fields and the pulse durations during writing and erasing, strange recovery in various quanti ties has been found out. The phenomenon can be explained by the change in the surface states density during the cycles. Practical importance of the finding is to offer some possibility to fabricate non-volatile random access memory without limitation to the cycles.

References

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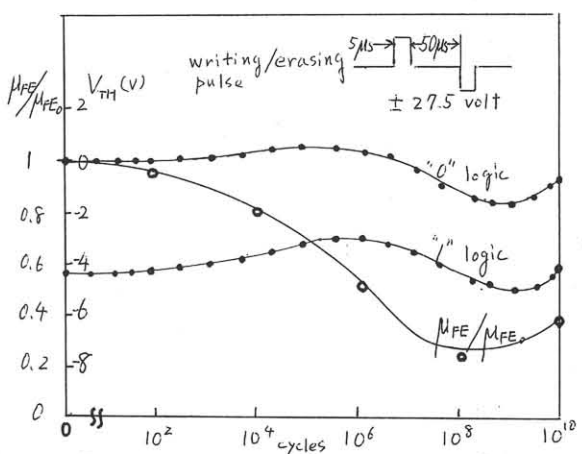

Fig.1. Mobility and Threshold Voltage

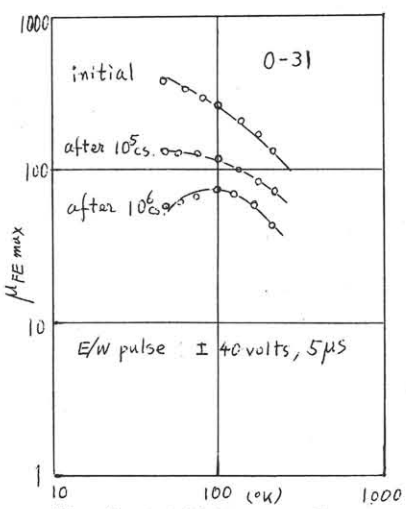

Fig.2. Mobility vs. T