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B5-3 A 1Kb N-Silicon-Gate Static Random-Acess Memory with Two Different Depletion-Load Thresholds

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Recently MOS random-access memories (RAM's) have been investigated extensively. Dynamic type aims at high memory density because of its advantages of fewer transistors per memory cell and lower power dissipations, compared with static type. On the other hand, static RAM's have been widely used due to their ease in use since they operate with a single low supply voltage and fully DC stable (static) circuitry and therefore need no complex timing and refreshing circuitry.

This paper describes a 1024-bit (quad 256) static MOS RAM with a small power-delay product (250mW x 300nsec) and other features (Fig. 1). In order to achieve a fast access time, n-channel silicon gate technology has been employed in combination with enhancement/depletion (E/D) circuit configuration on high resistivity (20 ohm-cm) p-type silicon wafers (Fig. 2). In general, n-channel silicon gate processes are more complicated than p-channel. In the device fabrication, a new process was employed which provides a self-aligned structure and reduces two photolithographic and one ion implantation steps.

Threshold voltages (turn-one voltages) of both enhancement-mode and depletion-mode transistors were controlled by ion implantation of boron and phosphorus, respectively. Typical values are V_{thE}=0.8V and V_{thD1}=-2.8V.

Power dissipation was attempted to be reduced mainly in the memory array without any sacrifice of access time and array size. An acess time of high bit-density static RAM's is determined mainly by switching speed in the decoder and input/output buffer circuits. Therefore the reduction of the power dissipation of the peripheral circuits always results in a slower access time. The power dissipation in the memory cell, however, can be reduced to a value enough for stable storing of written informations, without an increase in access time. This was achieved by a different threshold voltage of the depletion loads V_{thD2}=-1.2V in the memory cells with an additional merit of reduction in cell size. Other methods lead to a larger cell size or a complicated fabrication process.

Another important problem for RAM's is to elimenate completely a sneak path between two or more storage cells. At the transient time of cell selection, two cells are possibly selected simultaneously. To avoid this phenomenon, new simple decoder circuits have been developed, which will be published in details at the conference.

Fig. 3 shows oscillograph traces of the address and output signals.

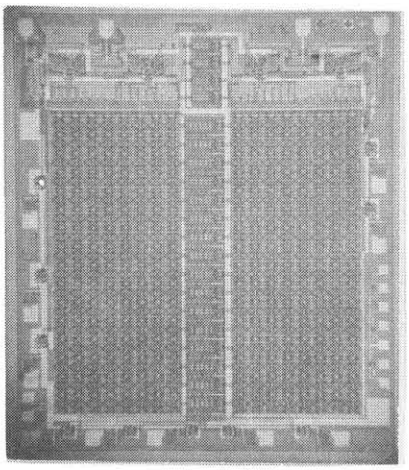

Fig. 1 Photograph of 1Kb static RAM.
(Chip Size : 3.1×3.5mm^2)

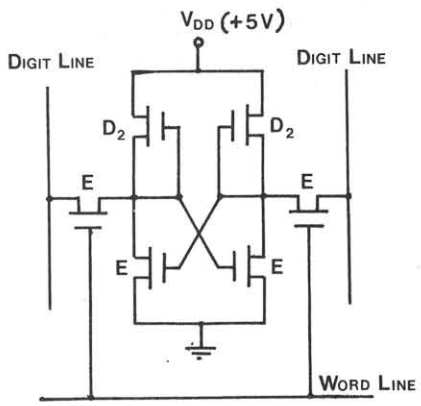

Fig. 2 Circuit of memory cell.

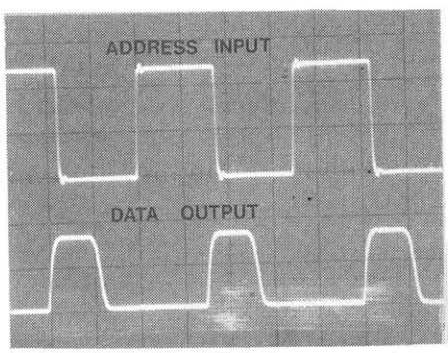

Fig. 3 Address input and data output signals.
Horizontal : 200nsec/div. , Vertical : 2V/div.
(Single power supply : +5V)