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B6-1 (INVITED) Logic Circuits with 2μm Gate Schottky Barrier FETs*

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The improvement of the performances of the one chip CPU has currently been pursued. Major problems are to realize high-speed logic gate circuits with sufficiently small power dissipation and to integrate them into large scale devices ($10^3 \sim 10^4$ gates/chip).

The power dissipation of the conventional high speed logic circuits (10∿100 mW/gate) is too large to the application and is required to be reduced by about two orders without deterioration of their speed. To overcome this problem, many attempts have been reported. DSA ED MOS IC,[1] IIL[2] and CMOS/SOS IC are considered as promising ones.

In this paper, fabrications and performances of a femto-joule logic circuits with the enhancement type Schottky barrier FET (ESB FET) are described.

The structure of the ESB FET is shown in Fig. 1. The active n-layer was formed by implanting $^{31}P^+$ ions into p^--silicon substrate (V_{ac}=80 kV, ϕ=1.4x10^{12} cm^{-3}). The PtSi-Si system was used as the Schottky contact in the gate (ϕ_B=0.82 eV) as well as ohmic ones in the n^+ source and drain regions. The threshold voltage was satisfactorily controlled in the range 0.07 ± 0.02 volts (enhancement mode) by controlling the thickness of the PtSi layer and the doping in the implanted n-region.

The DC characteristics of the ESB FET with 2μm gate is shown in Fig. 2. The performances observed in the device (V_{th}=0.05 volts) are g_{ms}=5m℧/mm (V_{GS}=0.4 volts) and C_G=0.9 pF/mm.

Four basic logic circuits (DCTL, DL, DTL and DDL) were designed using the ESB FETs, Schottky diodes and implanted layer resistors (Fig. 3). In order to evaluate the dynamic performances of the circuits, they were integrated to fifteen stage ring oscillators with output buffers.

The ring oscillators could be operated with a power supply as low as $V_{DD} \gtrsim 1$ volt. The oscillation waveforms of DCTL circuit are shown in Fig. 4. The delay and power dissipation of the four basic circuits are compared in Fig. 5. The merit factors (delay x power) of the DCTL circuit are found in the range 50 fJ (t_{pd}=5 ns, P=0.01 mW, V_{DD}=1 volt) ∼ 1 pJ (t_{pd}=1 ns, P=1 mW, V_{DD}=3 volts).

The effects of the increased F/I and/or F/O on the delay were also evaluated experimentally and the delay was given as $t_{pd}(m,n)/t_{pd}(1,1) = 1 + 0.15(m-1) + 0.7(n-1)$ in the DCTL circuits

with F/I=m and F/O=n.

The logic swing of 0.4 volts gives a favorable compatibility with the low level CML. The noise margin is estimated to be about 30 % of the logic swing under reasonable operating conditions.

The improved performances and the well controllable fabrication processes will suggest the promising feasibility of the device in the advanced LSI Logic application.

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1) Y. Tarui, et al., Proceedings of the 2nd Conference on Solid State Devices, Tokyo. Supplement to the Jour. of the Japan Soc. of Appl. Physics 40, 193, 1971.
2) H. Berger, et al, IEEE J. of Solid-state circuits SC-7, 340, 1972.

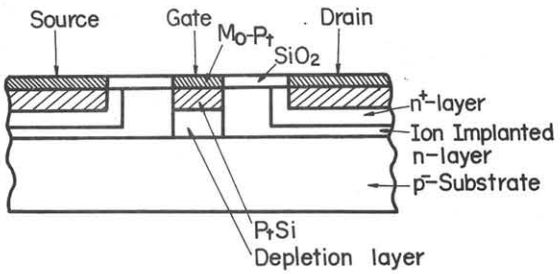

Fig.1 Cross section of a ESBFET.

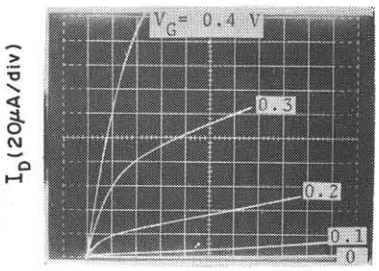

Fig.2 DC characteristics of a ESBFET having 2μm gate length and 300μm gate width.

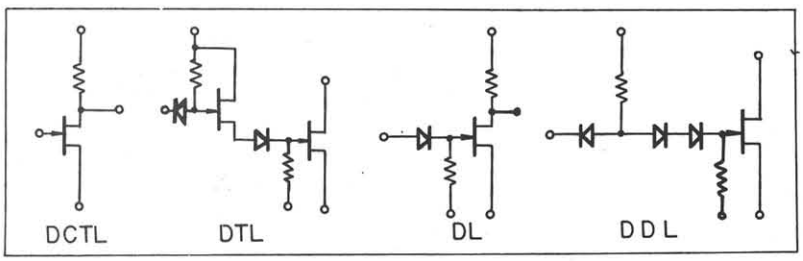

Fig.3 Basic logic circuits using the ESBFET.

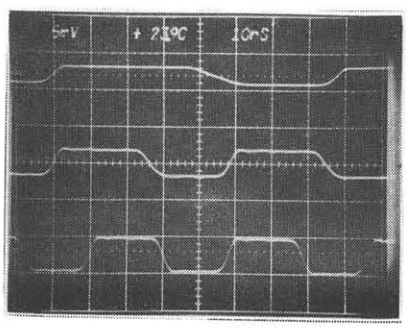

Fig.4 Out put wave forms of a 15-stage ring oscillator using DCTL.

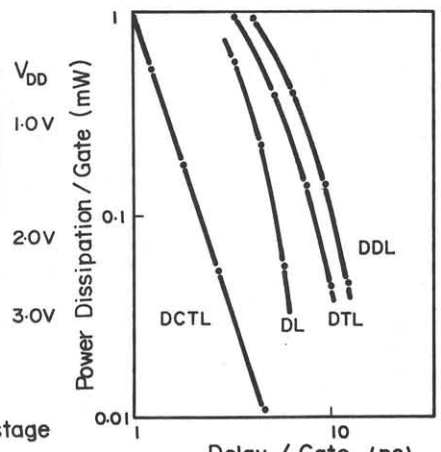

Fig.5 Power-delay curves for four different Type of logic gate.