Digest of Tech. Papers The 6th Conf. on Solid State Devices, Tokyo, Sep. 1974

B6-5 Device Design of an Ion Implanted High Voltage MOSFET

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The high voltage MOSFET with an ion implanted offset gate structure having some 300 volts was proposed by Erb and Dill[1] and also attempted by the authors[2]. In the device, the offset gate region is qualitatively considered to play a role of reducing the electric field around the drain edge. However, no theoretical treatments have been done for the device design. In this paper an analytical model is proposed for the full understanding of the device operation and for the optimization of the implanted region for any given geometical structures.

As shown in Fig.1, the model consists of a pinched resistor for the implanted region and a conventional MOSFET for the active channel region. The I-V characteristics of the device were obtained from the I-V equations of the both elements based on the gradual approximation. The impurity profile in the implanted region was assumed as a step one. As the drain voltage V_D increases, the voltage V_M at the node M becomes pinned at a certain voltage V_{Mmax} due to the pinch-off of the implanted region. Thus the first key parameter is V_{Mmax}, which is given by

$$V_{Mmax} = \frac{q}{2\epsilon_S} \cdot \frac{N_B N_R + N_R^2}{N_B} \cdot d^2 - \phi_B \ , \quad N_R = N_{DS} / d \qquad (1)$$

where q is electronic charge, ϵ_S is dielectric constant of Si, N_B is doping density of the substrate, N_R, N_{DS} and d are doping density, ion dose in Si and the depth of the implanted region. ϕ_B is the potential barrier between the substrate and the implanted region.

Fig.2 shows the dependence of V_{Mmax} on N_{DS} for n-type substrates, which was calculated from equation (1). In order to increase the drain breakdown voltage V_{DB} of the device, V_{Mmax} should be controlled within the breakdown voltage V_{CB}, 80 volts, of the conventional MOSFET with a drain doping density of $2\times10^{16}cm^{-3}$. The upper limit of N_{DS} is obtained from the cross points in Fig.2, where $V_{Mmax} = V_{CB}$.

On the other hand, the lower limit of N_{DS} is given by the critical gate voltage V_{GC}, the second parameter, above which the drain current ceases to increase due to the pinch-off of the resistor. The drain current or V_{GC} should be determined from the current handling capability of the device. Fig.3 shows the calculated V_{GC} as a function of N_{DS}. Using Fig.3 the optimum range of N_{DS} for p-channel high voltage MOSFET's can be calculated.

To confirm the device model, p-channel devices were

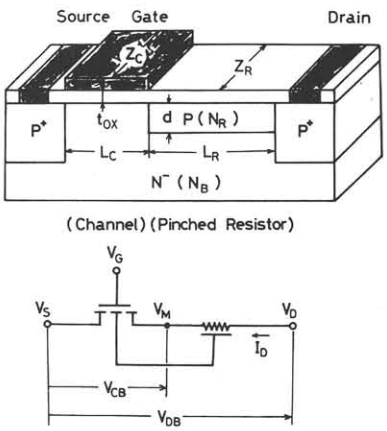

Fig.1 Schematic construction and equivalent circuit of the high voltage MOSFET.

fabricated using n-type Si of 7 ohm cm (N_B=7x10^{14}cm^{-3}). $^{11}B^+$ was implanted at an energy of 30 keV to a dose of 3 ~ 20x10^{11}cm^{-2}, followed by the annealing at 950 °C. The length of the pinched resistor L_R and the active channel L_C are 25 μm and 20 μm.

As shown in Fig.4, the I-V characteristics of the fabricated devices were in good agreement with those computed on the basis of the model. The analysis indicates that in the condition above the optimum range of N_{DS} to attain the device capable of both high voltage and sufficient current with V_{GC} =10 volts are in 5.8 ~ 8.4x10^{11}cm^{-2}.

The analytical model of the high voltage MOSFET described in the paper can also provide the precise design condition for the device geometries L_R and L_C.

References

(1) D.M.Erb and H.G.Dill ; IEDM, 21-4 (1971).

(2) I.Yoshida and T.Tokuyama ; IECE Japan, SSD73-14 (1973).

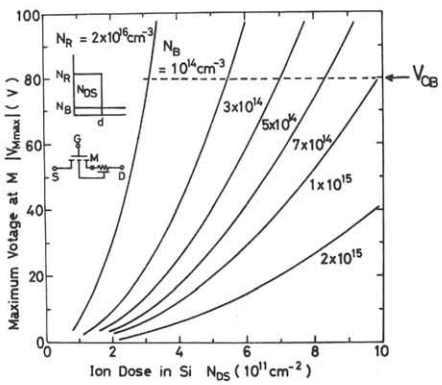

Fig.2 Calculated V_{Mmax} as a function of N_{DS}.

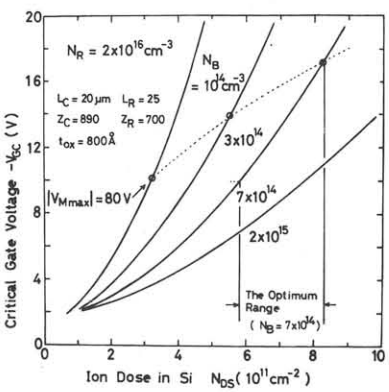

Fig.3 Calculated V_{GC} as a function of N_{DS} for the p-channel high voltage MOSFET's.

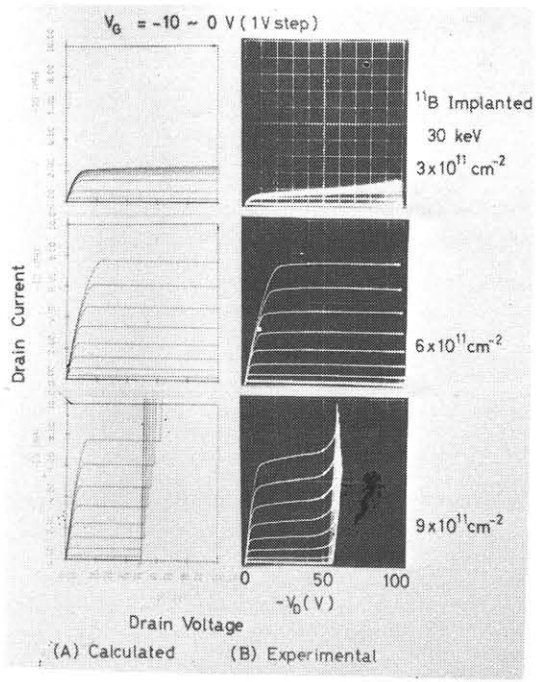

Fig.4 Computed and experimental I_D-V_D characteristics of the p-channel high voltage MOSFET's for different implanted doses.