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A-2-1 Semi-Insulating Polycrystalline-Silicon (SIPOS) Passivation Technology

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The surface-passivation technology for semiconductors has been developed. This technology has brought about a fundamental solution to a weakness of the planar method. This technology provides much higher reliability than the former method, and at the same time the production cost of devices can be reduced. This method can be applied to the mass production of nearly all types of silicon devices and integrated circuits.

Also the technology makes it possible to produce transistors capable of withstanding very high voltages, so that 10,000-volt devices can be stably manufactured, which has been considered difficult before. Futhermore, the packaging of elements can be greatly simplified.

The planar technology uses the thermal oxide. However, the charges on the outer surface of the oxide or within the oxide have influence on the interface charges of silicon substrates. Therefore, the characteristics of the planar devices depend on the charges on the outer surface of the oxide or within the oxide. Also the positive surface-state charge Q_{ss} exist in the interface between silicon and thermal oxide. Accordingly, PNP high voltage transistors have not been fabricated before by the planar technology.

On the other hand, the PN diodes passivated by undoped polycrystalline-silicon films have already been studied.1) These devices show much higher reliability than the planar devices. However, the diodes incur a considerable leakage-current under reverse biases.

Doping oxygen atoms into polycrystalline-silicon films has been attemped and the films have been applied to the surface passivation. Oxygen-doped polycrystalline-silicon films are far less conductive than undoped polycrystalline-silicon films and may be classified as semi-insulating films. Oxygen-doped polycrystalline-silicon has been named Semi-Insulating Polycrystalline-Silicon (SIPOS). Oxygen-doped polycrystalline-silicon films are deposited at 650°C from the SiH_4-N_2O-N_2 system and oxygen-concentration can be precisely controlled by changing the flow-rate ratio of N_2O to SiH_4 gas.

SIPOS films contain the traps of relatively higher density as compared with thermal oxide films in the forbidden gap. In SIPOS passivation for silicon devices, the charges on the outer surface of SIPOS film have influence on the charges of traps within SIPOS film, but not influence in the interface charges. Because of this protective feature of SIPOS films, only inexpensive coating need be used, eliminating expensive package and reducing the final size of the unit.

The interface states between SIPOS films containing 15 to 35 at. % oxygen and silicon substrates may act to inhibit the formation of the inversion layer in the surface region of both N- and P-type silicon substrates. Therefore, PNP high voltage transistors have been fabricated very easily.

The passivation properties of SIPOS films are examined and compared with undoped polycrystalline-silicon films and thermal oxide films used in the planar technology. Figure 1 shows the cross section of SIPOS transistor which SIPOS films are deposited directly with 0.5µm thickness on the surface of transistor after base and emitter have been diffused and thermal oxide removed. Figure 2 shows the linearity of h_{FE}. SIPOS films greatly improve the surface recombination velocity as compared with undoped polycrystalline-silicon films as shown in Figure 2. Figure 3 shows collector-base junction breakdown voltages of NPN transistors as a function of oxygen-concentration. The breakdown voltages decrease with increasing oxygen-concentration. Figure 4 shows collector-base reverse currents with emitter open as a function of oxygen-concentration. Figure 5 shows the collector-base reverse current of 10,000-volt NPN transistor with the double field-limiting ring structure.2) Figure 6 shows an example which the reliabilities of 800-volt PNP SIPOS transistors have been greatly improved. Therefore, SIPOS passivation technology is expected to open up a new field for semiconductors.

References: 1) Y. Kajiwara, S. Nagai and H. Hagino: 6 th symposium on Semiconductor, IC., April, 9(1974) Tokyo, Japan.
2) T. Matsushita and H. Hayashi: 1973 International Conf. on Solid State Devices, Paper 10-4, Tokyo, Aug. 31.

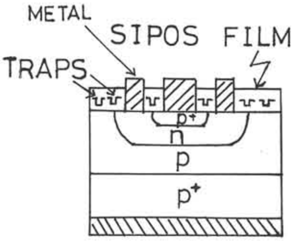

Fig.1. A cross section of SIPOS transistor.

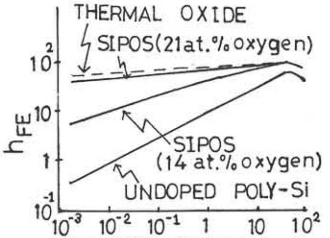

Fig.2. Linearity of h_{FE} of NPN transistor.

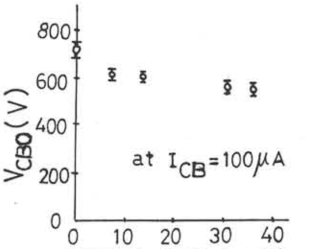

Fig.3. V_{CBO} vs oxygen conc.

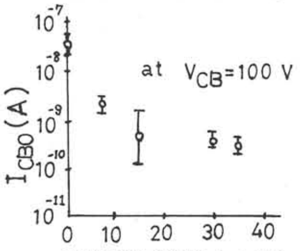

Fig.4. I_{CBO} vs oxygen conc.

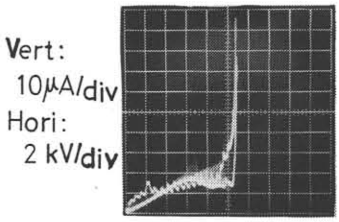

Fig.5. Collector-base reverse current of 10,000 V transistor.

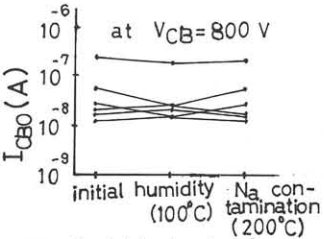

Fig.6. Life test of PNP transistor.