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A New Heterojunction-Gate GaAs FET

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A basic structure of GaAs J-FET having a heterojunction gate has been proposed by the present authors.[1] The gate region of the device is composed of multiepitaxial layers of n-GaAs, p-GaAlAs and p-GaAs, where the gate length is determined by the selective etching of p-GaAlAs. The potential advantage of the new structure over the conventional Schottky-barrier gate FET is that the fabrication process requires fewer masks because the selective etching of the heteroepitaxial layer is of great use for the self-aligned gate formation. In this paper, the structure and fabrication technology of a heterojunction-gate GaAs FET, which is composed of n-GaAs/p-GaAlAs/Ti, will be described in full detail.

A schematic cross section of the device is formed by the selective etching of p-GaAlAs with the mask of the uppermost film of titanium. This process provides a well-defined "mashroom" gate as shown in Fig. 2.

The active channel layer of the FET, the n-GaAs layer, was grown on a semi-insulating GaAs substrate from the vapour phase of the $(CH_3)_3Ga/AsH_3/H_2$ system[2] to a thickness of 0.5 μm being doped with selenium to a free carrier concentration of $5 \times 10^{16} cm^2/V \cdot s$. The gate consists of a heterojunction between this VPE n-GaAs layer and an overdeposited LPE p-GaAlAs layer of a thickness of 3 μm and of a free carrier concentration of $1 \times 10^{17} cm^{-3}$ or more. The titanium metal, for the mask during the subsequent selective etching, was evaporated on the top of the p-GaAlAs layer. For the active layer formation the vapour phase growth, especially the pyrolytic process using organic gallium, is preferable to the liquid phase growth. Autodoping of chromium from the semi-insulating substrate into the active layer is so remarkably suppressed in the pyrolytic process that a well-controlled impurity profile across the thin channel layer can be obtained. The fabrication procedures to complete the self-aligned gate are as follows. Using a photoresist mask, the film of titanium around the gate region was etched off with the dilute HF solution. The unwanted p-$Ga_{0.5}Al_{0.5}As$ layer was selectively etched in the hot solution of 1 HCl: 1 H_3PO_4 through the patterned titanium film. We have found that the proposed etching solution dissolves only $Ga_{0.5}Al_{0.5}As$ with an etching rate of 0.3 μm/min at 50°C, resulting in a mirror-like etched surface, while it attacks neither GaAs nor titanium. The "mashroom" structure thus obtained is of practical importance in the subsequent self-aligning procedure. Gold-germanium eutectic was evaporated and alloyed with GaAs at 500°C to form the ohmic contacts. The contact metal film deposited is automatically cut along the edge of the mashroom. The self-aligning technique was again used in the over-depositing process of aluminum for the lead connection. In our preliminary experiment using a mask of gate width/length of 400 μm/5 μm, the gate mashroom obtained was 2 μm in gate length with an approximately 1.5 μm undercut region.

A typical dc characteristic of the experimental transistor is shown in Fig. 3.

The transistor showed a drain current saturation of 45 mA at 3 V drain voltage for zero gate voltage. The pinch-off voltage and the transconductance of this device were found to be 3.5 V and 20 m℧, respectively. The reverse I-V characteristic of the gate junction is shown in Fig. 4, comparing with that of an Al-GaAs Schottky-barrier gate FET made from the same epitaxial wafer using the same masks. It is seen that the heterojunction gate has a lower leakage current than that of the Schottky-barrier gate FET.

The proposed structure and technology are promising in the realization of submicron gate FET's which can provide a new approach to the GaAs microwave transistors.

References

(1) S. Umebachi, K. Asahi, M. Inoue, and G. Kano; IEEE Trans. Electron Device, ED-22 (Aug. 1975) (To be published).

(2) M. Inoue and K. Asahi; Japan. J. appl. Phys., 11, 919 (1972).

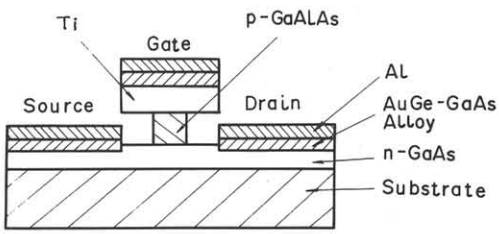

Fig. 1. Schematic cross section of the proposed heterojunction-gate GaAs FET.

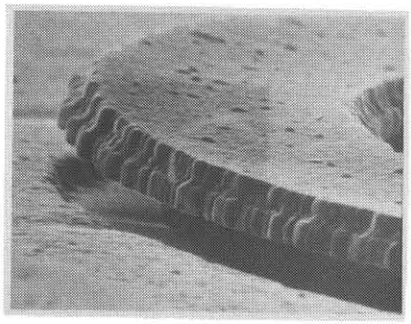

Fig. 2. An SEM photograph of the gate part.

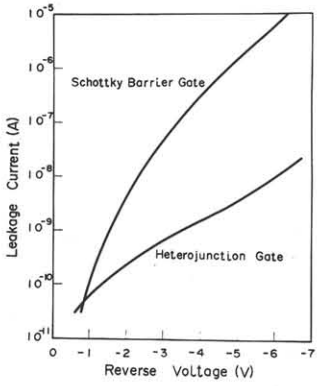

Fig. 4. An example of leakage characteristics of the heterojunction gate diode in comparison with that of a Schottky-barrier gate diode.

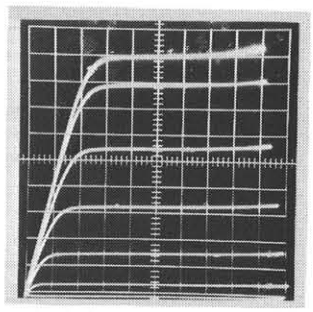

Fig. 3. A typical dc I-V characteristic of the heterojunction-gate GaAs FET. Gate length: 2/um. H: 1V/div. V: 5mA/div. Gate bias: 0.5V/step.