Digest of Tech. Papers The 7th Conf. on Solid State Devices, Tokyo, Sep. 1975

A-4-3 Two-dimensional Analysis of Vertical Junction-Gate FET's

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A vertical junction-gate FET (V-FET) with triode-like I-V characteristics was first proposed by Nishizawa.[1] Electrons injected into an intrinsic channel were considered to carry space-charge-limited current which was modulated by a p-i junction gate. Among the merits of the V-FET are: (1) high input and low output impedance, (2) high output voltages and (3) thermal stability due to the negative temperature coefficient of the majority carrier mobility. These features are of great advantage in linear circuit applications, especially audio power amplifiers[2].

There have been, however, few comprehensive theoretical studies done on the mechanism of the triode-like characteristics of FET's. The purpose of this work is to clarify the criteria for the triode-like operations of a junction-gate FET. It is also intended to provide the design principle of Si V-FET's including the breakdown limitations by means of a two-dimensional numerical analysis.

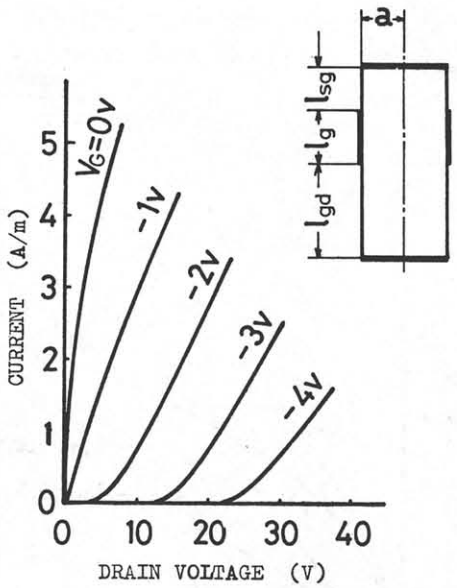


Fig.1 Current-voltage characteristics

For the mathematical model of V-FET we assume a symmetrical gate structure as shown in the inset of Fig.1. The basic equations for an n-channel V-FET operation, in conventional notations, are:

$$\nabla^2\psi = -\frac{q}{\varepsilon}\left(N_D - n\right), \qquad (1)$$

$$\frac{\partial n}{\partial t} = \nabla \cdot J \qquad (2)$$

where N_D is the donor impurity concentration. An electron drift velocity, which saturates at high electric field, is used.

Calculated current-voltage characteristics of a V-FET are shown in Fig.1. A triode-like characteristic is obtained when the (negative) gate bias is deeper than -1v.

Figure 2 shows the carrier concentration distributions, when V-FET operates as a triode (V_G=-3v). At this gate voltage, the channel is completely depleted. However, as the drain voltage is increased, the potential barrier in the channel is reduced resulting in increased carrier density (Fig.2(a)). When the drain

voltage is high enough, the potential barrier is finally flattened out and the carriers are allowed to flow through the channel (Fig.2(b)). The drain current increases as the drain bias is raised because of the increased number of carriers induced, giving to the triode-like characteristics (see Fig.1).

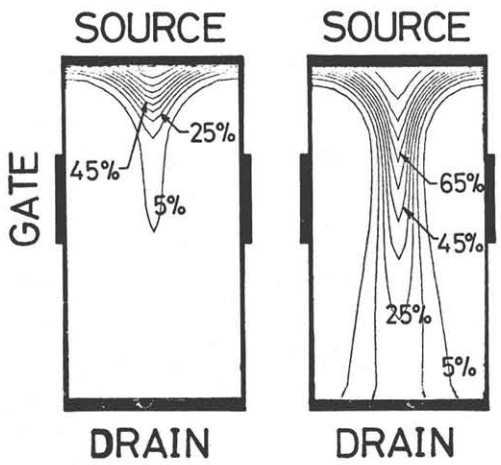
It should be apparent that a channel depleted by the gate potential is a prerequisite for a triode-like characteristics. This gives a limitation on N_D for a given channel thickness, 2a. More striking are the criteria on the gate length l_g and gate-to-drain distance, l_{gd}. For a larger l_{gd}, for example, the I-V characteristics are like those of a pentode, as shown in Fig.3. It is also found that there exists an upper bound on l_g, above which the drain voltage can no longer induce carriers in the channel. It is the virtue of the two-dimensional analysis that brings about these design criteria.

The breakdown voltage is determined by solving the Poisson's equation in two dimensions and by carrying out the ionization integral along the path of the highest electric field. Because of electric field crowding at the gate edges, the breakdown voltage is smaller than that of a one-dimensional one-sided abrupt junction.

Device parameters such as on-resistance R_{on}, transconductance g_m and breakdown voltage BV are obtained from the above analysis. The two-dimensional numerical approach is thus found to be a powerful tool in the design of V-FET's which show triode-like characteristics.

1) J.Nishizawa, Japanese Patent Publication No.6077 of 1953

2) Wireless World, 80, No.1463, 223(1974)



(a) V_D=15V (b) V_D=25V

Fig.2 Contour-line maps of electron density distribution

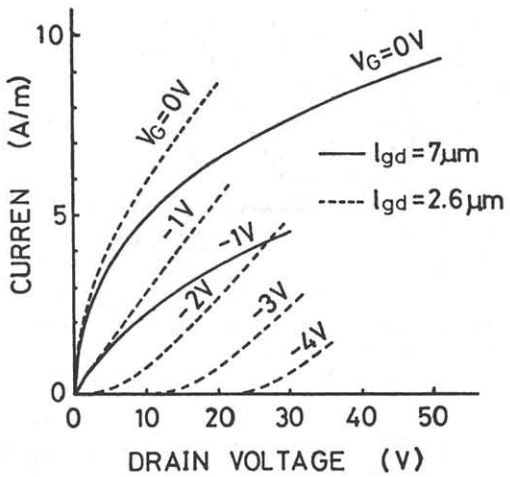


Fig.3 Current-voltage characteristics