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# A-5-1 Multi-Channel FET with A New Diffusion Type Structure

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Vertical type FETs have been reported in several structures. One is fabricated by epitaxial technology[1)2)3)] and the other is made by the local oxidation process.[4)]

This paper describes the design and performance of a multi-channel FET with a new planar structure, which can be fabricated using processes compatible with bipolar transistors.

The principle structure of this device is shown in Fig. 1. Mesh gate $P^+$ region and source $N^+$ regions are formed on the N-type epitaxial layer by conventional photolithographic techniques and mask diffusion techniques. This new structure brings about a vertical type FET suitable for both low-frequency high-power and microwave frequency applications.

Figure 2 shows the I-V characteristics of the 1.3 x 1.3 $mm^2$ chip device in this structure. It shows a voltage amplification factor of about 10 and good input-output linearity. These characteristics can be precisely determined by the gate diffusion process.

Figure 3 shows an advanced fabrication process suitable for high power devices. This structure does not require accurate mask alignments, and offers a high breakdown voltage of the source and gate junction. First, a p-type epitaxial layer is grown on the $P^+$ substrate. Then, the surface of the wafer is oxidized and both the gate diffusion window and the source contact holes are made in the first oxidation layer. Thin $Si_3N_4$ film is deposited on the surface and only the gate diffusion window portion is removed by the plasma etching technique (Fig. 3(a)). After the gate diffusion and oxidation, the $Si_3N_4$ film on the source contact holes is etched off. This self-aligning method is extremely important to get high source-gate breakdown voltage, because the nearest distance between them determines the punch-through type breakdown voltage. The surface is covered with a heavily Boron-doped polycrystalline silicon film (Fig. 3(c)). The low resistance polycrystalline silicon is essential to prevent for the source metal to touch the electric field of the reverse biased gate junction. All the polycrystalline silicon, except the source electrode region, is removed by the plasma etching process. After the gate contact hole is made in the $SiO_2$ film, the source and gate metal electrodes are attached to the device by the final process (Fig. 3(d)).

Figure 4 shows the output I-V characteristics of a 5520-channel power FET. The output impedance ranges from 3 to 15 Ω and the voltage amplification factor is approximately 5. This device can deliver a 50 W signal to an 8 Ω load impedance output stage of a push-pull class-B amplifier.

This structure is also suitable for microwave frequency applications. The cut-off frequency of FET is limited by two factors, one is input port RC time constant and the other is channel transit time. In this structure, reduction of the former can be attained by decreasing the gate resistance. The gate impurity concentration can be made high to its solubility limit, or a metal electrode can be laid on the whole gate region. The latter can be reduced by thin epitaxy and a shallow gate diffusion.

The device with a refined pattern was fabricated in 0.4 x 0.4 $mm^2$ chip whose structure was shown in Fig. 1. Figure 5 shows the input-output characteristics. Output power of 1 W, 3 db gain and 30% efficiency were observed at 900 MHz.

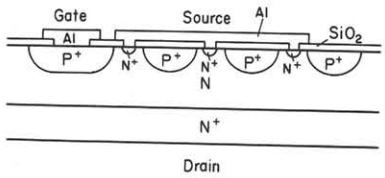


Fig. 1 Diffusion type vertical FET.

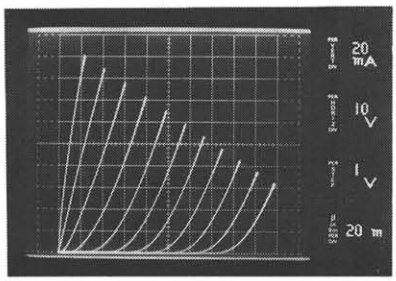


**Fig. 2 I-V characteristics of 1.3 x 1.3 $mm^2$ chip device.**

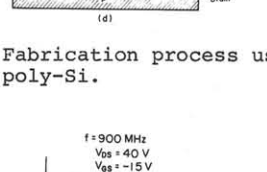


Fig. 3 Fabrication process using poly-Si.

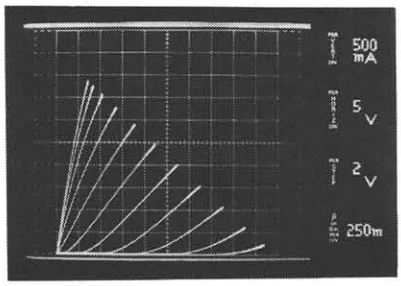


**Fig. 4 I-V characteristics of power device.**

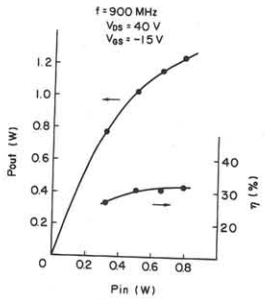


Fig. 5 High frequency characteristics.


(1) J. Nishizawa et al RIEC Technical Report TR-36 (1973)
(2) K. Sakai et al PESC 74 Record p.214 (1974)
(3) O. Ozawa et al 35th Meeting of JSAP p.247 (1974)
(4) A. Ishitani et al Japan IECE Meeting p.271 (1975)